High-Performance Non-PCI 32-bit 10/100/1000M Gigabit Ethernet Controller

Document No: AX88180/V1.10

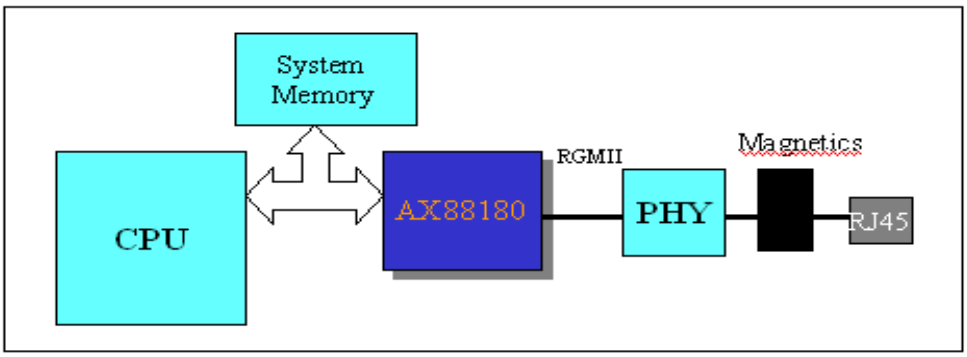
Features

- High-performance non-PCI local bus
  - 16/32-bit SRAM-like host interface (US Patent Approval)
  - Support big/little endian data bus type
  - Large embedded SRAM for packet buffers
    - 32K bytes for receive buffer
    - 8K bytes for transmit buffer
  - Support IP/TCP/UDP checksum offloads
  - Support interrupt with high or low active trigger mode
- Highly-integrated Gigabit Ethernet controller
  - Compatible with IEEE802.3, 802.3u, and 802.3ab standards
  - Support 10/100/1000Mbps data rate
  - Support full duplex operation with 1000Mbps data rate
  - Support full and half duplex operations with 10/100Mbps date rate
  - Support 10/100/1000Mbps N-way Auto-negotiation operation
  - Support IEEE 802.3x flow control for full-duplex operation
  - Support 10/100/1000Mbps data rate with RGMII or MII in 10/100Mbps data rate.
  - Support back-pressure flow control for half-duplex operation
  - Support packet length set by software
  - Support max 4K bytes JUMBO packet
- Support Wake-on-LAN function by following events
  - Detection of network link-up state
  - Receipt of a Magic Packet
- Support Magic Packet detection for remote wake-up after power–on reset
- Support EEPROM interface
- Support synchronous or asynchronous mode to host MCU
- Integrated voltage regulator from 3.3V to 2.5V
- 2.5V for core and 3.3V I/O with 5V tolerance
- 128-pin LQFP with CMOS process, RoHS package

Product Description

The AX88180 is a high-performance and cost-effective non-PCI Gigabit Ethernet controller for various embedded systems including consumer electronics and home network markets that require a higher bandwidth of network connectivity. The AX88180 supports 16/32-bit SRAM-like host interface and Gigabit Ethernet MAC, which is IEEE802.3 10Base-T, IEEE802.3u 100Base-T, and IEEE802.3ab 1000Base-T compatible. The AX88180 supports full-duplex or half-duplex operation at 10/100Mbps speed and supports full-duplex operation at 1000Mbps speed. The AX88180 integrates large embedded SRAM for packet buffers to accommodate high bandwidth applications and supports IP/TCP/UDP checksum to offload processing loading from microprocessor/microcontroller in an embedded system

System Block Diagram



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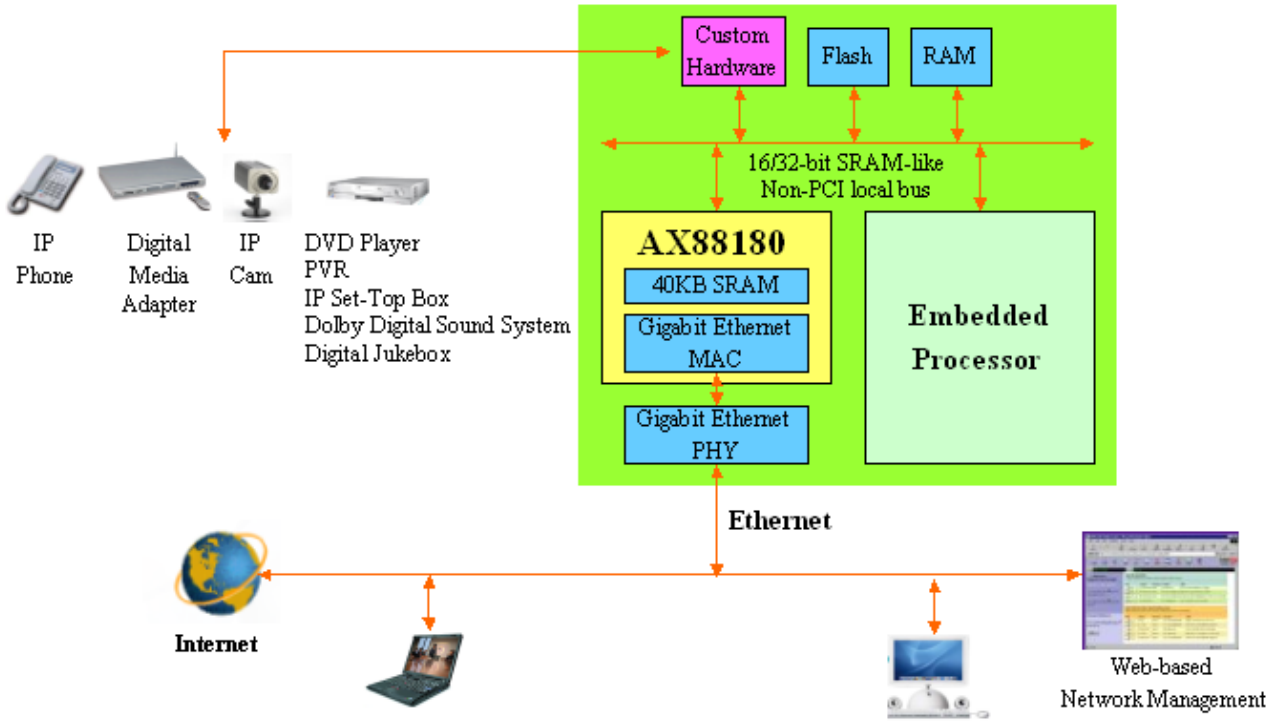
Target Applications

- Multimedia applications
  - Content distribution application
    - Audio distribution system (Whole-house audio)
    - Video-over IP solutions, IP PBX and video phone
    - Video distribution system, multi-room PVR
  - Cable, satellite, and IP set-top box
  - Digital video recorder
  - DVD recorder/player
  - High definition TV
  - Digital media client/server
  - Home gateway
  - IPTV for triple play
- Others
  - Printer, kiosk, security system
  - Wireless router & access point

Applications

The AX88180, design with a high-performance RISC CPU, provides a very low cost yet very high-performance embedded networking solution to enable easy and simple LAN or Internet access capability to high-bandwidth multimedia application needs in the Internet era.



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1.0 Introduction

1.1 General Description

The AX88180, SRAM-like 16/32-bit local bus to Gigabit Ethernet bridge, supports a 10/100/1000 Mbps with RGMII (V2.0 in delay timing) or MII in wire-speed operation. AX88180 supports RGMII (802.3ab, 1000Base-T) interface with full-duplex operation at gigabit speed and full-duplex or half-duplex operation at 10/100 Mbps speed. AX88180 can also operate in MII mode with 10/100Mbps speed.

The AX88180 has two built-in synchronous SRAM for buffering packet. The one is 32K bytes for receiving packets from Ethernet PHY; the other is 8K-bytes for transmitting packets from host system to Ethernet PHY. The AX88180 also has 256 bytes built-in configuration registers. For software programming, the total address space used in AX88180 is 64K in 32-bit mode and at least (8K + 8) bytes in 16-bit mode.

Because AX88180 is a SRAM-like device, AX88180 could be treated as a SRAM device and can be attached to SRAM controller of system. Therefore, system can execute DMA cycles to gain the highest performance.

AX88180 needs 2 clock sources. One (HCLK) is the same to host system clock or from stand-along OSC, the other is 125Mhz (CLK125) for AX88180 running in RGMII mode. In general application, the 125MHz clock can be from Giga -PHY for cost effectively.

1.2 AX88180 Block Diagram

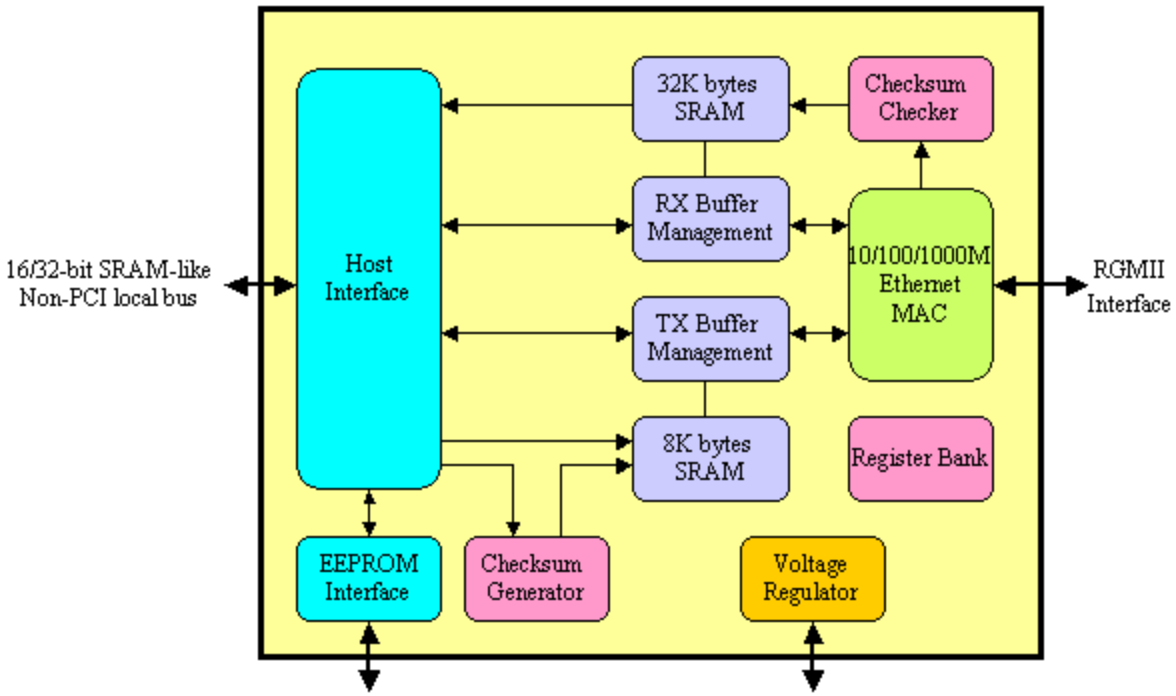


Figure 1. AX88180 block diagram

1.3 AX88180 Pinout Diagram

The AX88180 is housed in the 128-pin LQFP package.

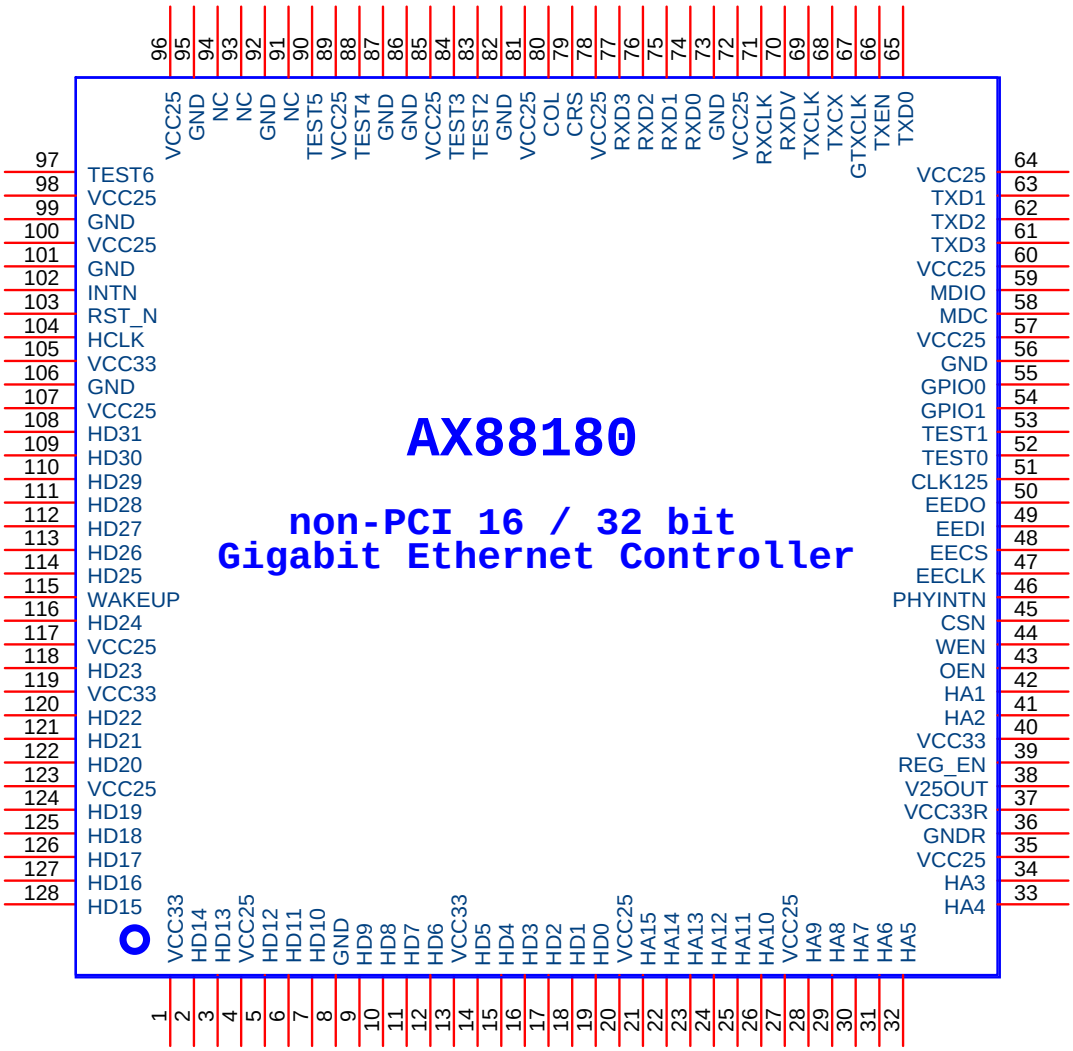


Figure 2. AX88180 pin connection diagram

2.0 Signal Description

2.1 Signal Type Definition

I3: Input, 3.3V with 5V tolerance
I2: Input, 2.5V with 3.3V tolerance
I25 Input 2.5V only
O3: Output, 3.3V
O2: Output, 2.5V
IO3: Input/Output, input 3.3V with 5V tolerance
IO2: Input/Output, input 2.5V with 3.3V tolerance
TSO: Tri-State Output
OD: Open Drain allows multiple devices to share as a wire-OR
PD: Internal 75K Pull Down
PU: Internal 75K Pull Up
GND: Digital Ground
VCC3: 3.3V power
VCC2: 2.5V power
I: Input only
O: Output only
IO: Input/Output

2.2 RGMII/MII Interface

Table 1. RGMII/MII Interface signals group

Pin Name	Type	Pin NO	Pin Description
CLK125	I3	51	Free running clock 125MHz from OSC or Giga-PHY in RGMII mode. This pin should be pulled down in MII mode.
TXEN	O2, 12mA	66	Transmit Enable: TXEN is transition synchronously with respect to the rising and falling edge of TXCX. TXEN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
TXD[3:0]	O2, 12mA	61,62,63,65	Transmit Data: TXD[3:0] is transition synchronously with respect to the rising and falling edge of TXCX. In rising edge TXD[3:0] is as general TD[3:0] and falling edge TXD[3:0] is as TD[7:4]. TD[7:0] is used in AX88180 as byte unit.
TXCX	O2, 12mA	68	2.5M/25M/125MHz Clock Output in RGMII mode: It is a continuous 2.5M/25M/125MHz clock output to Giga-PHY for 10/100/1000Mbps operations respectively in RGMII mode. It is a timing reference for TXEN and TXD[3:0]. For normal operation, this pin should be connected to Giga-PHY in RGMII mode and should be floating in MII mode.
GTXCLK	O2, 12mA	67	125MHz Clock Output: It is a continuous 125 MHz clock output. This pin is for internal debug purpose only and should be floating for normal operation.
RXCLK	I2	71	Receive Clock: RXCLK is a continuous clock that provides the timing reference for RXDV, RXD[3:0]. This clock is provided from PHY.
RXD[3:0]	I2	77,76,75,74	Receive Data: RXD[3:0] is driven by the PHY synchronously with respect to RXCLK. In rising edge RXD[3:0] is as RD[3:0] and falling edge is as RD[7:4]. RD[7:0] is used in AX88180 as byte unit.
RXDV	I2	70	Receive Data Valid: RXDV is driven by the PHY synchronously with respect to RXCLK in rising and falling edge. It is asserted high when valid data is present on RXD [3:0].

COL	I2	80	Collision: This signal is driven by PHY when collision is detected.
CRS	I2	79	Carrier Sense: Asynchronous signal CRS is asserted by the PHY when either the transmitted or receive medium is non-idle.
MDIO	IO2, PU, 8mA	59	Station Management Data Input /Output: Serial data input/Output transfers from/to the PHY. The transfer protocol conforms to the IEEE 802.3u MII specification.
MDC	O2, 8mA	58	Station Management Data Clock: The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock.
PHYINTN	I2	46	Interrupt signal from PHY, active low.
TXCLK	I2	69	A clock from Giga-PHY operates in MII mode. If the Giga-PHY provides the clock source for 10/100Mbps operations in MII mode, AX88180 can use this pin as reference clock. In this case, this pin should be connected to the TXCLK pin of Giga-PHY in MII mode. This pin should be pulled down in RGMII mode.

2.3 Host Interface

Table 2. Host Interface signals group

Pin Name	Type	Pin NO	Pin Description
INTN	TSO, 8mA	102	Interrupt to host system When the polarity is active high, this signal must be pulled low, otherwise pulled high in active low environment. Software set the bit6 of command register (CMD) to response the polarity.
RST_N	I3	103	Reset signal: active low.
HCLK	I3	104	Reference Clock. This clock may be from host (synchronous mode) or the output of stand-alone OSC (asynchronous mode). The HCLK clock signals MUST be provided synchronously for AX88180 synchronous reset and hardware configuration during booting up the system. Please refer to Appendix A3 for more details of system design considerations.
WAKEUP	TSO, 8mA	115	Wake-up signal to system. When the polarity of system is active high, this signal must be pulled low, otherwise pulled high in active low environment. Software set the bit0 of command register (CMD) to response the polarity.
HD0	IO3, 8mA	19	Data bus bit0.
HD1	IO3, 8mA	18	Data bus bit1.
HD2	IO3, 8mA	17	Data bus bit2.
HD3	IO3, 8mA	16	Data bus bit3.
HD4	IO3, 8mA	15	Data bus bit4.
HD5	IO3, 8mA	14	Data bus bit5.
HD6	IO3, 8mA	12	Data bus bit6.
HD7	IO3, 8mA	11	Data bus bit7.
HD8	IO3, 8mA	10	Data bus bit8.
HD9	IO3, 8mA	9	Data bus bit9.
HD10	IO3, 8mA	7	Data bus bit10.
HD11	IO3, 8mA	6	Data bus bit11.
HD12	IO3, 8mA	5	Data bus bit12.
HD13	IO3, 8mA	3	Data bus bit13.
HD14	IO3, 8mA	2	Data bus bit14.
HD15	IO3, 8mA	128	Data bus bit15.
HD16	IO3, 8mA	127	Data bus bit16, internal pull down. *
HD17	IO3, 8mA	126	Data bus bit17, internal pull down. *
HD18	IO3, 8mA	125	Data bus bit18, internal pull down. *

HD19	IO3, 8mA	124	Data bus bit19, internal pull down. *
HD20	IO3, 8mA	122	Data bus bit20, internal pull down. *
HD21	IO3, 8mA	121	Data bus bit21, internal pull down. *
HD22	IO3, 8mA	120	Data bus bit22, internal pull down. *
HD23	IO3, 8mA	118	Data bus bit23, internal pull down. *
HD24	IO3, 8mA	116	Data bus bit24, internal pull down. *
HD25	IO3, 8mA	114	Data bus bit25, internal pull down. *
HD26	IO3, 8mA	113	Data bus bit26, internal pull down. *
HD27	IO3, 8mA	112	Data bus bit27, internal pull down. *
HD28	IO3, 8mA	111	Data bus bit28, internal pull down. *
HD29	IO3, 8mA	110	Data bus bit29, internal pull down. *
HD30	IO3, 8mA	109	Data bus bit30, internal pull down. *
HD31	IO3, 8mA	108	Data bus bit31, internal pull down. *
HA1	I3	42	Address bus bit1.
HA2	I3	41	Address bus bit2.
HA3	I3	34	Address bus bit3.
HA4	I3	33	Address bus bit4.
HA5	I3	32	Address bus bit5.
HA6	I3	31	Address bus bit6.
HA7	I3	30	Address bus bit7.
HA8	I3	29	Address bus bit8.
HA9	I3	28	Address bus bit9.
HA10	I3	26	Address bus bit10.
HA11	I3	25	Address bus bit11.
HA12	I3	24	Address bus bit12.
HA13	I3	23	Address bus bit13.
HA14	I3	22	Address bus bit14.
HA15	I3	21	Address bus bit15.
WEN	I3	44	Data Write Enable: Host drives WEN and it is active low.
CSN	I3	45	Chip Select Enable. Host drives CSN and it is active low.
OEN	I3	43	Data Output Enable: Host drives OEN and it is active low.

*Note: The internal Pull-down of HD16 to HD31 will be disabled in 32-bit mode.

2.4 EEPROM Interface

Table 3. EEPROM Interface signals group

Pin Name	Type	Pin No.	Pin Description
EECLK	O3, 12mA	47	A low speed clock to EEPROM
EECS	O3, 12mA	48	Chip select to EEPROM device.
EEDI	O3, 12mA	49	Data to EEPROM, valid in EECS is high and EECLK in rising edge.
EEDO	I3, PD	50	Data from EEPROM

2.5 Regulator Interface

Table 4. Regulator signals group

Pin Name	Type	Pin No.	Pin Description
VCC33R	VCC3	37	3.3V power to internal regulator
GNDR	GND	36	Ground pin for internal regulator
REG_EN	I3	39	High to enable internal regulator. Low to disable internal regulator.
V25OUT	O2	38	2.5V output from internal regulator, max 250mA, when REG_EN pin is high.

2.6 Miscellaneous

Table 5. Miscellaneous signals group

Pin Name	Type	Pin No.	Pin Description
GPIO0	IO3, 12mA, PD	55	General Purpose pin. In reset stage this pin defines chip operates in 16 or 32-bit mode. Pull-down is for 32-bit mode and pull-up (by 4.7K) is for 16-bit mode. If this pin is floating, it will be as default for 32-bit mode.
GPIO1	IO3, 12mA, PD	54	General Purpose pin. In reset stage this pin defines chip operates in little-endian or big-endian mode. Pull-down is little-endian mode and pull-up is big-endian mode. If this pin is floating, it will as default for little-endian mode.
TEST0	I3, PD	52	Connect to ground or floating for normal operation.
TEST1	I3, PD	53	Connect to ground or floating for normal operation.
TEST2	I25	83	Pull-down (by 4.7K) to ground for normal operation.
TEST3	I25	84	Pull-down (by 4.7K) to ground for normal operation.
TEST4	I25	88	Pull-down (by 47K) to ground for normal operation
TEST5	I25	90	Connect to ground for normal operation.
TEST6	I25	97	Pull-up (with 4.7K) to VCC25 for normal operation
NC	O	91,93,94	No connection

2.7 Power/ground pin

Table 6. Power/Ground pins group

Pin Name	Type	Pin No.	Pin Description
VCC33	VCC3	1,13,40, 105, 119	3.3V power pins
VCC25	VCC2	4,20,27,35,57,60,64,72,78,81,85,89,96,98,100,107, 117,123	2.5V power pins
GND	GND	8,56,73,82,86,87,92,95,99,101,106	Ground pins

3.0 Functional Description

3.1 Host Interface

AX88180 supports a very simple SRAM-like interface. There are only 3 control signals to operate the read or write. For write operation, host activates CSN and WEN to low with address and data bus. AX88180 will decode and latched the data into internal buffer. For normal operation, the WEN needs at least 4 clocks duration for one 32/16-bit write operation. The CSN can always be driven, but WEN must at least be de-asserted 1 clock before next access. For read operation, host asserts CSN and OEN at least 5 clocks to AX88180, the data will be valid after 4 clocks. AX88180 also support burst mode if host reads/writes AX88180 by continuous access. Note: The burst mode only supports in TX/RX, not supports in registers read/write. That is, reads RX area from XXXX_0000 to XXXX_7FFF or writes TX area from XXXX_8000 to XXXX_FBFF can be accessed by burst mechanism.

3.2 System Address Range

AX88180 is suitable to attach to SRAM controller, so it needs 64K memory space for operation. The designer can allocate any block (64K) in system space. From offset 0x0000 to 0x7FFF is for RX operation, and offset 0x8000 to 0xFBFF is for TX operation. The internal configuration register of AX88180 is allocated in offset 0xFC00 to 0xFCFF. Below is the mapping of addressing.

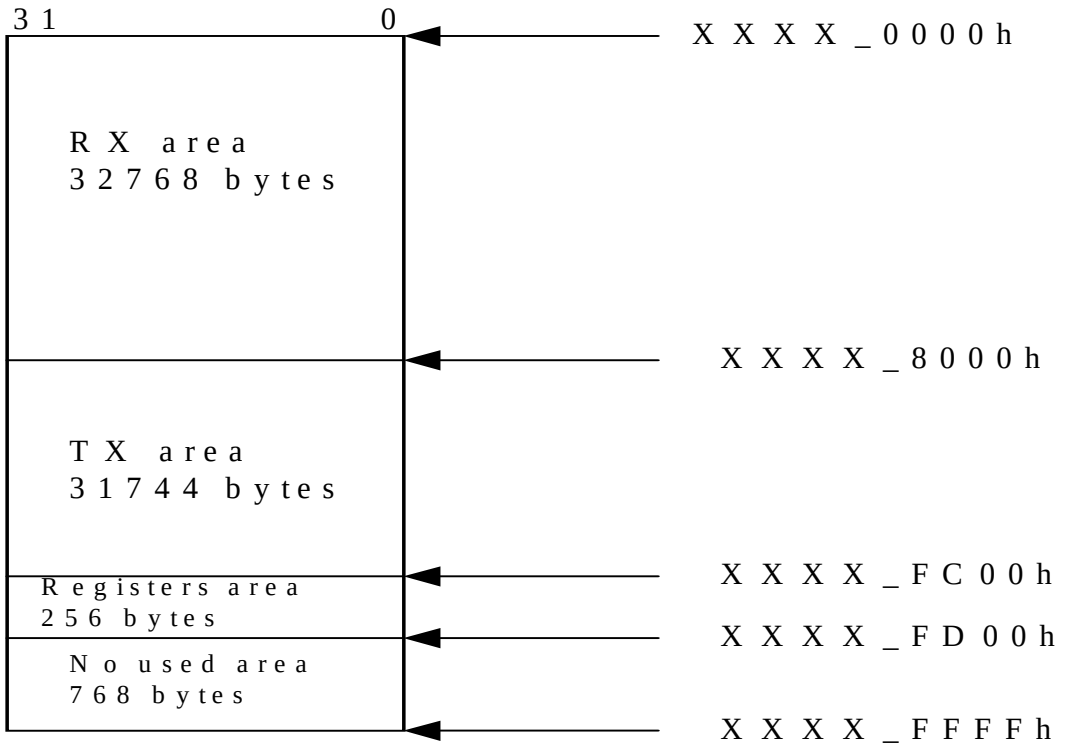


Figure 3. 32-bit mode address mapping

3.3 TX Buffer Operation

AX88180 employs 4 descriptors to maintain transmit information, such as packet length, start bit. These descriptors are located in offset 0xFC20, 0xFC24, 0xFC28 and 0xFC2C. Driver can choose any descriptor whenever there is data needed to be transmitted. Since there are only 4 descriptors, upon running out of descriptors, driver must wait for the descriptor is to be released by AX88180.

3.4 RX Buffer Operation

AX88180 is built a 32K SRAM for RX operation. It utilizes ring structure to maintain the input data from PHY and read out to host. There are two pointer registers located in offset 0xFC34 and oxFC38. AX88180 will maintain RXCURT register. Upon it receives a valid packet from PHY it will update RXCURT according to the packet length. Driver reads data from AX88180 and maintains the RXBOUND register. When driver finishes reading packet, it must update RXBOUND according to the packet length. AX88180 utilizes RXCURT and RXBOUND to provide receive buffer status, full or empty.

3.5 Flow Control

In full duplex mode, AX88180 supports the standard flow control mechanism defined in IEEE 802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When space of the packet buffer is less than the threshold values (RXBTHD0, RXBTHD1), AX88180 will send out a PAUSE-ON packet to stop the remote node transmission. And then AX88180 will send out a PAUSE-OFF packet to inform the remote node to retransmit packet if it has enough space to receive packets.

3.6 Checksum Offloads and Wake-up

To reduce the computing loading of CPU, AX88180 is built checksum operator for IP, UDP or TCP packet. AX88180 will detect the packet whether it is IP, UDP or TCP packet. If it is an IP packet, AX88180 will calculate the checksum of header and put the result in checksum filed of IP. Then it continuously checks the packet whether it is UDP or TCP. It will perform the checksum operation whenever it is a UDP or TCP packet. AX88180 also automatically skip the VLAN tag when checksum is executed. AX88180 also supports to detect magic packet or link-up to wake up system when system is in sleep state or needs to cold start by magic packet.

3.7 Burst-Mode support

To improve the throughput in embedded system, AX88180 supports fast-mode (burst) for TX/RX buffer access. Host can access AX88180 by driving CSN to low and toggle WEN (write) or OEN (read). AX88180 can support the burst until whole packet access. The access timing can refer to section 5.5.4 and 5.5.6. This mechanism is only for TX/RX buffer access. For configuration register access, it must use single access.

3.8 Big/Little-endian support

AX88180 supports “Big” or “Little” endian data format. The default is Little-endian. Designer can pull-up GPIO1 pin to high to swap the data format. Below table can depict the relation.

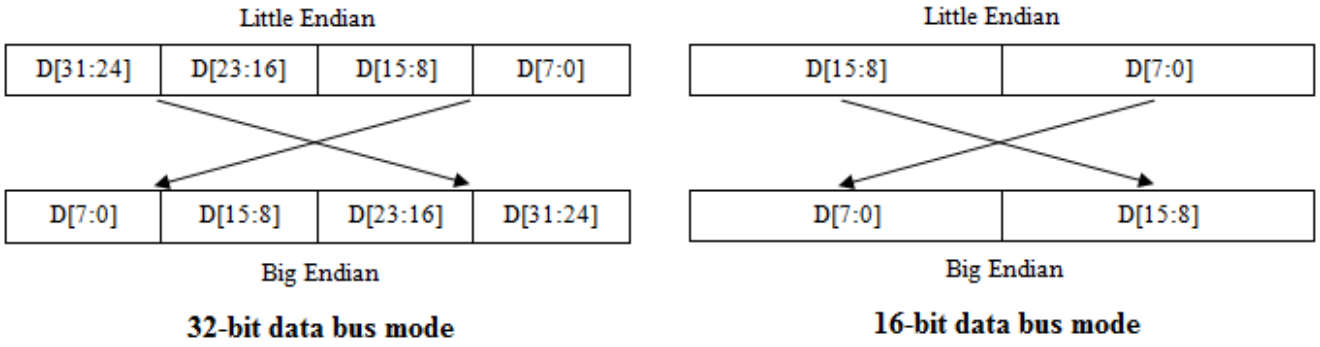


Figure 4. data swap block

3.9 16-bit Mode

AX88180 also supports 16-bit mode operation. AX88180 driver should request at least (8K + 8) bytes space for TX, RX and register access. For example, the driver requests a 16K bytes space from system and then sets the new window base address to MEMBAS6 register. After that, driver should set bit 0 (DECODE_EN) of MEMBASE register to start decoding for TX buffer, RX buffer and registers access. (Note: AX88180 H/W only decodes low 16-bit offset address.)

MEMBASE--Memory base Address

Field	Name	Type	Default	Description
15:1	-	R/W	-	Reserved. The output value is undefined if software read this field.
0	DECODE_EN	R/W	0	16-bit decode enable Set to '1' to start decoding.

MEMBAS6--Memory base Address + 6

Field	Name	Type	Default	Description
15:8	-	R/W	-	Reserved. The output value is undefined if software read this field.
7:0	WINSIZE	R/W	0x00	Window Base Pointer. (The MSB of new window base address, 16-bit offset) This field defines another new windows base address for TX, RX and register access. The total size is 8K bytes. TX areas occupy 3840 bytes Registers occupy 256 bytes. RX areas occupy 4096 bytes.

Note: The WINSIZE field of this address is used to define the MSB of new window base address, the TX buffer, RX buffer and registers should be accessed through this new window base address in 16-bit mode. Please refer to below mapping mechanism for details.

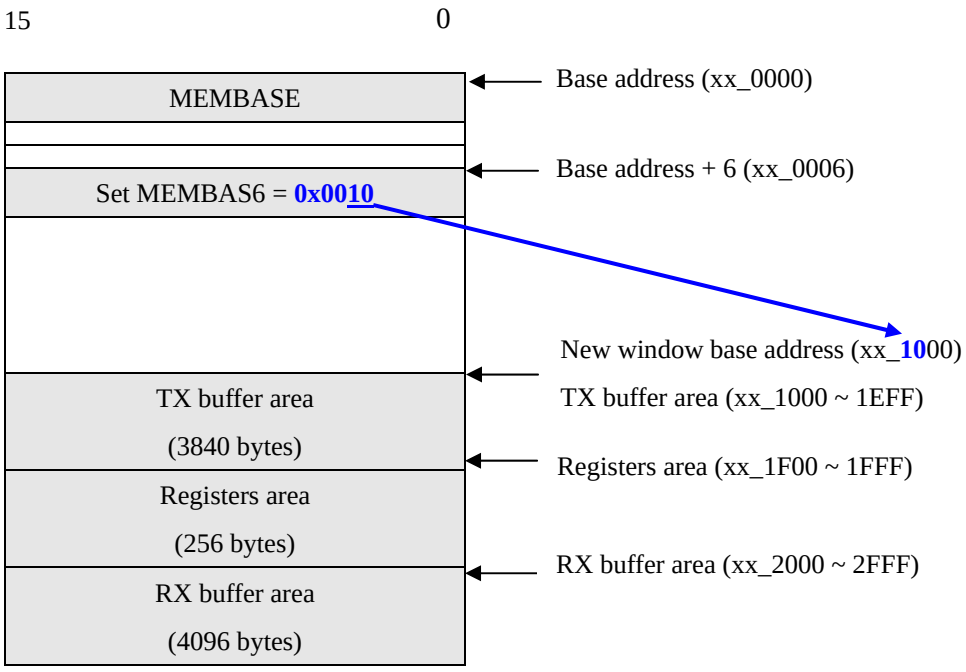


Figure 5. 16-bit mode memory mapping

The following is an example to indicate how to define a new window base address in 16-bit mode by configuring the MEMBAS6 register. If AX88180 is allocated at the memory base address 0x20_0000 by hardware (i.e. the MEMBASE register is allocated at 0x20_0000) and users would like to set the new window base address to 0x20_1000, the driver should write 0x0010 to the MEMBAS6 register (offset 0x20_0006). In this case, the TX buffer area will be allocated from 0x20_1000 to 0x20_1EFF; the registers area will be allocated from 0x20_1F00 to 0x20_1FFF and the RX buffer area will be allocated from 0x20_2000 to 0x20_2FFF. (Note: AX88180 only decodes low 16-bit address)

3.10 EEPROM Format

AX88180 supports 16-bit data access serial EEPROM device like 93C56 EEPROM. AX88180 will auto-load data from EEPROM device after hardware reset. If the EEPROM device is not attached, the loading operation will be discarded. The EEPROM mainly provides MAC address information and the following table is the format if EEPROM device is employed.
Note: If the MAC address is 12-34-56-78-9A-BC then driver should set MACID0=0x3412, MACID1=0x7856 and MACID2=0xBC9A.

Address	16-bits data Description
0	Must be set 0x0070. This field should not be set to 0x0000 or 0xFFFF; otherwise, AX88180 will not recognize the EEPROM during hardware reset.
1	MACID0 data
2	MACID1 data
3	MACID2 data
4	Reserved, keep all 0's
5	Bit0: must be '0' Bit1: must be '0' Bit2: 1 = set RGMII mode by EEPROM, 0 = none. (The setting will be cleared when software resets) Bit3: 1 = set Gigabit mode by EEPROM, 0=none (The setting will be cleared when software resets) Others bits must set to 0s
6 ~ 127	Reserved, keep all 0's

4.0 Register Description

There are some registers located from 0xFC00 to 0xFCFF. All of the registers are 32-bit boundary alignment, but only low 16-bit are available (exception 0xFC54). For reserved bits, don't set them in normal operation.

Table 7. MAC Register Mapping

Offset	Name	Description	Default value
0xFC00	CMD	Command Register	0x0000_0201
0xFC04	IMR	Interrupt Mask Register	0x0000_0000
0xFC08	ISR	Interrupt Status Register	0x0000_0000
0xFC10	TX_CFG	TX Configuration Register	0x0000_0040
0xFC14	TX_CMD	TX Command Register	0x0000_0000
0xFC18	TXBS	TX Buffer Status Register	0x0000_0000
0xFC20	TXDES0	TX Descriptor0 Register	0x0000_0000
0xFC24	TXDES1	TX Descriptor1 Register	0x0000_0000
0xFC28	TXDES2	TX Descriptor2 Register	0x0000_0000
0xFC2C	TXDES3	TX Descriptor3 Register	0x0000_0000
0xFC30	RX_CFG	RX Configuration Register	0x0000_0101
0xFC34	RXCURT	RX Current Pointer Register	0x0000_0000
0xFC38	RXBOUND	RX Boundary Pointer Register	0x0000_07FF
0xFC40	MAC_CFG0	MAC Configuration0 Register	0x0000_8157
0xFC44	MAC_CFG1	MAC Configuration1 Register	0x0000_6000
0xFC48	MAC_CFG2	MAC Configuration2 Register	0x0000_0100
0xFC4C	MAC_CFG3	MAC Configuration3 Register	0x0000_060E
0xFC54	TXPAUT	TX Pause Time Register	0x001F_E000
0xFC58	RXBTHD0	RX Buffer Threshold0 Register	0x0000_0300
0xFC5C	RXBTHD1	RX Buffer Threshold1 Register	0x0000_0600
0xFC60	RXFULTHD	RX Buffer Full Threshold Register	0x0000_0100
0xFC68	MISC	Misc. Control Register	0x0000_0013
0xFC70	MACID0	MAC ID0 Register*	0x0000_0000
0xFC74	MACID1	MAC ID1 Register*	0x0000_0000
0xFC78	MACID2	MAC ID2 Register*	0x0000_0000
0xFC7C	TXLEN	TX Length Register	0x0000_05FC
0xFC80	RXFILTER	RX Packet Filter Register	0x0000_0004
0xFC84	MDIOCTRL	MDIO Control Register	0x0000_0000
0xFC88	MDIODP	MDIO Data Port Register	0x0000_0000
0xFC8C	GPIO_CTRL	GPIO Control Register*	0x0000_0003
0xFC90	RXINDICATOR	Receive Indicator Register	0x0000_0000
0xFC94	TXST	TX Status Register	0x0000_0000
0xFCA0	MDCLKPAT	MDC Clock Pattern Register	0x0000_8040
0xFCA4	RXCHKSUMCNT	RX IP/UDP/TCP Checksum Error Counter	0x0000_0000
0xFCA8	RXCRCNT	RX CRC Error Counter	0x0000_0000
0xFCAC	TXFAILCNT	TX Fail Counter	0x0000_0000
0xFCB0	PROMDPR	EEPROM Data Port Register	0x0000_0000
0xFCB4	PROMCTRL	EEPROM Control Register	0x0000_0000
0xFCB8	MAXRXLEN	MAX. RX packet Length Register	0x0000_0600
0xFCC0	HASHTAB0	Hash Table0 Register*	0x0000_0000
0xFCC4	HASHTAB1	Hash Table1 Register*	0x0000_0000
0xFCC8	HASHTAB2	Hash Table2 Register*	0x0000_0000
0xFCCC	HASHTAB3	Hash Table3 Register*	0x0000_0000
0xFCE0	DOGTHD0	Watch Dog Timer Threshold0 Register	0x0000_FFFF
0xFCE4	DOGTHD1	Watch Dog Timer Threshold1 Register	0x0000_0000
0xFCEC	SOFTRST	Software Reset Register	0x0000_0003

***Note: It is not affected by software reset**

4.1 CMD--Command Register

Offset Address = 0xFC00 Default = 0x0000_0201

Field	Name	Type	Default	Description
31:16	-	R/W	All 0's	Reserved
15	RXVLAN	R/W	0	RX VLAN indicator Driver enables this bit to indicate AX88180 that the received packet will include 4 bytes VLAN tag; AX88180 will skip 4 bytes when it calculates the checksum of IP, TCP or UDP packet. 1 = enable 0 = disable
14	TXVLAN	R/W	0	TX VLAN indicator Driver enables this bit to indicate AX88180 that the transmitted packet will include 4 bytes VLAN tag; AX88180 will skip 4 bytes when it calculates the checksum of IP, TCP or UDP packet. 1 = enable 0 = disable
13:10	-	R/W	All 0's	Reserved
9	RXEN	R/W	1	RX Function Enable When this bit is enabled, MAC starts to receive packets. 1 = enable 0 = disable
8	TXEN	R/W	0	TX Function Enable When this bit is enabled, MAC could start to transmit packet to Ethernet. 1 = enable 0 = disable
7	-	R/W	0	Reserved
6	INTMOD	R/W	0	Interrupt Active Mode Driver sets this bit to indicate AX88180 the interrupt of system is activated high or low. 1: Active high 0: Active low
5:1	-	R/W	All 0's	Reserved
0	WAKEMOD	R/W	1	WAKEUP pin polarity Driver sets this bit to indicate AX88180 the polarity of system wake-up signal is activated high or low. 1: Active high 0: Active low

4.2 IMR--Interrupt Mask Register

Offset Address = 0xFC04 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	PHYMASK	R/W	0	PHY interrupt Mask When this bit is enabled, an interrupt request from PHY set in bit 5 of Interrupt Status Register will make AX88180 to issue an interrupt to host. 1 = enable 0 = disable
4	PRIM	R/W	0	Packet Received Interrupt Mask When this bit is enabled, a received interrupt request set in bit 4 of Interrupt Status Register will make AX88180 to issue an interrupt to host. 1 = enable 0 = disable
3	PTIM	R/W	0	Packet Transmitted Interrupt Mask When this bit is enabled, a transmitted interrupt request set in bit 3 of Interrupt Status Register will make AX88180 issue an interrupt to host.

				1 = enable 0 = disable
2	-	R/W	0	Reserved
1	DOGIM	R/W	0	Watch Dog Timer Interrupt Mask When this bit is enabled, a watch dog timer expired interrupt request set in bit1 of Interrupt Status Register will make AX88180 to issue an interrupt to host 1 = enable 0 = disable
0	RXFULIM	R/W	0	RX Buffer Full Interrupt Mask When this bit is enabled, a RX buffer full interrupt request set in bit 0 of Interrupt Status Register will make AX88180 to issue an interrupt to host. 1 = enable 0 = disable

4.3 ISR--Interrupt Status Register

Offset Address = 0xFC08 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	PHYIG	R/W	0	PHY Interrupt Generation If this bit is set to '1', it means there is an interrupt request from PHY. AX88180 will forward this interrupt to system. Meantime driver should poll PHY and adopt proper procedure. Write '1' to this bit to clear this request status. 1 = have interrupt request 0 = no interrupt request
4	RPIG	R/W	0	Receive Packet Interrupt Generation If this bit is set to '1', it means AX88180 receives a packet or (packets) from PHY. The packet is kept in RX buffer. Write '1' to this bit to clear this request status. 1 = have received packet 0 = no received packet
3	FTPI	R/W	0	Finish Transmitting Packet Interrupt If this bit is set to '1', it means AX88180 had transmitted packet to PHY. Write '1' to this bit to clear this request status. 1 = finish transmission 0 = none
2	-	R/W	0	Reserved
1	WDTEI	R/W	0	Watch Dog Timer Expired Interrupt If this bit is set to '1', it means the WATCH DOG timer is expired. AX88180 will issue an interrupt to host. Write '1' to this bit to clear this request status. The expired duration can refer to DOGTHD0 and DOGTHD1 registers. 1 = timer expired happens 0 = none
0	RXFULI	R/W	0	RX Buffer Full Interrupt If this bit is set to '1' it means RX buffer is full and no more packets will be received until packets are read out. Write '1' to this bit to clear this request status. 1 = RX buffer full 0 = None

4.4 TX_CFG--TX Configuration Register

Offset Address = 0xFC10 Default = 0x0000_0040

Field	Name	Type	Default	Description
31:7	-	R	All 0's	Reserved
6	TXCRCAP	R/W	1	TXCRC Auto-Append When this bit is enabled, AX88180 will append CRC to the transmitted packet in FCS field. 1 = enable 0 = disable
5	-	R/W	0	Reserved.
4	TXCHKSUM	R/W	0	TX Checksum Generation When this bit is enabled, AX88180 will append checksum to the transmitted packet that is IP or TCP or UDP packet. 1 = enable 0 = disable
3:2	-	R	00	Reserved
1:0	TXDS	R	00	TX Description Status AX88180 reports which descriptor is transmitted now Default: 2'b00

4.5 TX_CMD--TX Command Register

Offset Address = 0xFC14 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	HWI	R/W	0	Host Writes Indication Before host begins to send a packet to TX buffer, this bit should be set. At the end of host writes the packet, this bit should be cleared by software. 1 = Start Writing 0 = End Writing
14:13	TXDP	R/W	00	TX Descriptor Pointer To specify which TX descriptor to be written.
12	-	R/W	0	Reserved
11:0	DATALEN	R/W	All 0's	Byte Count. Data length is written to transmitted buffer.

4.6 TXBS--TX Buffer Status Register

Offset Address = 0xFC18 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:4	-	R	All 0's	Reserved
8	INTXDS	R	0	Internal TX descriptor status. This bit reports the TX descriptor status. When there is data to be transmitted, this bit will be set to '1' otherwise it will be '0' 1 = have data in TX buffer 0 = all data are transmitted to PHY
7:6	-	R	00	Reserved
5:4	TXDUSE	R	00	TX Descriptor In Transmitting These status bits indicate which descriptor is transmitting now. 00: Descriptor 0 in transmitting 01: Descriptor 1 in transmitting 10: Descriptor 2 in transmitting 11: Descriptor 3 in transmitting
3	TXD3O	R	0	TX Descriptor 3 Occupied This bit reflects bit 15 of TXDES3 register to indicate that it had used TX

				descriptor3. When the transmission is finished, AX88180 will auto-clear this bit.
2	TXD2O	R	0	TX Descriptor 2 Occupied This bit reflects bit 15 of TXDES2 register to indicate that it had used TX descriptor2. When the transmission is finished, AX88180 will auto-clear this bit.
1	TXD1O	R	0	TX Descriptor 1 Occupied This bit reflects bit 15 of TXDES1 register to indicate that it had used TX descriptor1. When the transmission is finished, AX88180 will auto-clear this bit.
0	TXD0O	R	0	TX Descriptor 0 Occupied This bit reflects bit 15 of TXDES0 register to indicate that it had used TX descriptor0. When the transmission is finished, AX88180 will auto-clear this bit.

4.7 TXDES0--TX Descriptor0 Register

Offset Address = 0xFC20 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD0_EN	R/W	0	Transmit TX descriptor 0 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, driver had already written data that is assigned to TX descriptor0 to TX buffer. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD0_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88180 how many bytes will be transmitted.

4.8 TXDES1--TX Descriptor1 Register

Offset Address = 0xFC24 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD1_EN	R/W	0	Transmit TX descriptor 1 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, driver had already written data that is assigned to TX descriptor1 to TX buffer. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD1_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88180 how many bytes will be transmitted.

4.9 TXDES2--TX Descriptor2 Register

Offset Address = 0xFC28 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD2_EN	R/W	0	Transmit TX descriptor 2 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, driver had already written data that is assigned to TX descriptor2 to TX buffer. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD2_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88180 how many bytes will be transmitted.

4.10 TXDES3--TX Descriptor3 Register

Offset Address = 0xFC2C Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD3_EN	R/W	0	Transmit TX descriptor 3 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, driver had already written data that is assigned to TX descriptor3 to TX buffer. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD3_LEN	R/W	All 0's	TX Packet Length (unit: byte) Driver set this field to indicate AX88180 how many bytes will be transmitted.

4.11 RX_CFG--RX Configuration Register

Offset Address = 0xFC30 Default = 0x0000_0101

Field	Name	Type	Default	Description
31:9	-	R	All 0's	Reserved
8	RXBME	R/W	1	RX Buffer Monitor Enable When this bit is enabled, MAC will monitor the status of receive buffer. 1 = enable 0 = disable
7:5	-	R/W	000	Reserved.
4	RXCHKSUM	R/W	0	RX Packet TCP/IP Checksum When this bit is set, AX88180 will check the checksum of the received packet that is IP, TCP or UDP packet. If there is checksum error, AX88180 will drop the packet and RXCHKSUMCNT counter will add 1. 1 = enable 0 = disable
3:1	-	R/W	000	Reserved
0	RXBUFPRO	R/W	1	RX Buffer Protection When this bit is enabled, MAC will protect the RX buffer to avoid overrun. For normal operation, this bit should be enabled in initial stage. 1= enable 0= disable

4.12 RXCURT--RX Current Pointer Register

Offset Address = 0xFC34 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXCURPTR	R/W	All 0's	RX Line Current Pointer. Point to the last line that will be written by hardware. The unit of line is 16 bytes. AX88180 will maintain this register.

4.13 RXBOUND--RX Boundary Pointer Register

Offset Address = 0xFC38 Default = 0x0000_07FF

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXBUNPTR	R/W	0x7FF	RX Line Boundary Pointer. Point to the last line that has been read by driver. The unit of line is 16 bytes. When driver finished reading packet from RX buffer, it must update this field.

4.14 MAC_CFG0--MAC Configuration0 Register

Offset Address = 0xFC40 Default = 0x0000_8157

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	SPEED100	R/W	1	Line Speed Mode When this bit is enabled and bit12 of MAC_CFG1 is disabled, MAC will operate in 100Mbps mode otherwise it operates in 10Mbps speed. If bit12 of MAC_CFG1 is enabled, this bit will be ignored
14	-	R/W	0	Reserved, this bit must set to 0 for normal operation
13	-	R/W	0	Reserved, this bit must set to 0 for normal operation.
12	RXFLOW	R/W	0	RX Flow Control If this bit and bit8 of RX_CFG are enabled, MAC will perform flow control and send pause on/off frame when the available space of receive buffer is less than the value of RXBTHD0. 1 = enable 0 = disable
11	-	R/W	0	Reserved, this bit must set to 0 for normal operation.
10:4	IPG100	R/W	0x15	Inter Packet Gap (IPG) for 10/100M This field defines the back-to-back transmit packet gap for 10/100M.
3:0	IPG1000	R/W	0x7	Inter Packet Gap for 1000M This field defines the back-to-back transmit packet gap for 1000M only.

4.15 MAC_CFG1--MAC Configuration1 Register

Offset Address = 0xFC44 Default = 0x0000_6000

Field	Name	Type	Default	Description
31:15	-	R	All 0's	Reserved
14	PUSRULE	R/W	1	Pause Frame Check Rule When this bit is set, AX88180 accepts pause frame that DA can be any value. 1 = don't check DA field. 0 = check DA is equal to "01 80 C2 00 00 01"
13	CRCCHK	R/W	1	Check CRC of received Packet. When this bit is enabled, AX88180 will drop any CRC error packet.

				1 = enable 0 = disable
12	GIGA_EN	R/W	0	Gigabit Mode Enable When this bit is enabled, MAC will operate in 1000Mbps mode. 1 = enable 0 = disable
11	RXJUMBO	R/W	0	RX Jumbo Enable When this bit is enabled, MAC will receive jumbo package 1 = enable 0 = disable
10:7	RXJUBOLEN	R/W	0000	Length Limit of received Jumbo package This field defines the maximum length of received jumbo package. 0001: 1K bytes 0010: 2K bytes 0011: 3K bytes ---------- 1110: 14K bytes 1111: 15K bytes
6	DUPLEX	R/W	0	Duplex Mode. 1 = Full-Duplex mode 0 = Half-Duplex mode
5	TXFLW_EN	R/W	0	TX Flow Enable When this bit is enabled, MAC will block the transmitted operation when it captures pause frame from Ethernet. The re-transmission will be activated until the waiting time is expired. 1 = enable 0 = disable
4:2	-	R/W	000	Reserved, must set to ‘0s’ for normal operation
1	RGMIIEN	R/W	0	RGMII Mode Enable When this bit is enabled, AX88180 will operate in RGMII interface. Driver must set external PHY to RGMII mode and enable this bit in initial stage. Driver also must set RGMII interface of external PHY with add-delay timing in its internal. 1 = enable 0 = disable
0	-	R/W	0	Reserved, must set to ‘0s’ for normal operation

4.16 MAC_CFG2--MAC Configuration2 Register

Offset Address = 0xFC48 Default = 0x0000_0100

Field	Name	Type	Default	Description
15:8	-	R/W	0x01	Reserved, keep this field in default value for normal operation.
7:2	JamLT	R/W	000000	Define Jam Limit for backpressure collision account. Normally set this field at 0x19. It can avoid HUB port going to partition state due to too many collisions. AX88180 will skip one frame collision backpressure when collision counter equal to JamLT. The collision count will be reset to zero when every transmit frame with no collision or receive a frame with no backpressure collision.
1:0	-	R/W	00	Reserved, must set to ‘00’ for normal operation

4.17 MAC_CFG3--MAC Configuration3 Register

Offset Address = 0xFC4C Default = 0x0000_060E

Field	Name	Type	Default	Description
15	NOABORT	R/W	0	No Abort When this bit is enabled, MAC will keep retry transmit current frame even excessive collision otherwise it will abort current transmission due to excessive collision. 1 = enable 0 = disable
13:7	IPGR1	R/W	0001100	Inter-Frame Gap segment1
6:0	IPGR2	R/W	0001110	Inter-Frame Gap segment2

4.18 TXPAUT--TX Pause Time Register

Offset Address= 0xFC54 Default = 0x001F_E000

Field	Name	Type	Default	Description
31:23	-	R	All 0's	Reserved
22:0	TXPVAL	R/W	0x1F_E000	TX Pause Time out It is used to re-transmit a pause-on frame when pause timer expired and receive buffer still not enough. In 32-bit mode, this field should be set to 0x1F_E000 at 1000Mbps mode and set to 0x7F_8000 at 10/100Mbps modes. In 16-bit mode, this field can be kept at the hardware default value 0x1F_E000 without writing this register at 10/100/1000Mbps modes. (Note: The bit 16 ~ 22 of this field are invalid in 16-bit mode written.)

4.19 RXBTHD0--RX buffer Threshold0 Register

Offset Address= 0xFC58 Default = 0x0000_0300

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXLOWB	R/W	0x300	RX Remainder Capacity Low-Bound This field defines as the remainder capacity of RX buffer for pause operation. If the flow control (bit12 of MAC_CFG0) is enabled, MAC will send pause frame when the available space of receive buffer is less than this value. The unit is 16-byte.

4.20 RXBTHD1--RX Buffer Threshold1 Register

Offset Address= 0xFC5C Default = 0x0000_0600

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXHIGHB	R/W	0x600	RX Remainder Capacity Upper-Bound This field defines as upper bound of remainder size of RX buffer for pause operation. If the flow control is enabled, MAC will stop to send pause frame until the available space of receive buffer is more than this value. The unit is 16-byte.

4.21 RXFULTHD--RX Buffer Full Threshold Register

Offset Address= 0xFC60 Default = 0x0000_0100

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXFULB	R/W	0x100	RX Full Threshold This field defines the least capacity of RX buffer. AX88180 will cause RX full if it remains capacity under this value. The unit is 16-byte.

4.22 MISC—Misc. Control Register

Offset Address= 0xFC68 Default = 0x0000_0013

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	WAKE_LNK	R/W	0	WAKE-UP by Link-Up Function If this bit is enabled, MAC will drive wakeup pin whenever there is link-up occurrence. The polarity of wakeup pin is according to bit0 of CMD register. 1= enable 0= disable
4	WAKE_MAG	R/W	1	WAKE-UP by Magic Packet If this bit is enabled, MAC will drive wakeup pin whenever there is magic packet detected by hardware. The polarity of wakeup pin is according to bit0 of CMD register. 1= enable wake-up by magic packet 0 = disable
3:2	-	R/W	00	Reserved
1	-	R/W	1	Reserved
0	SRST_MAC	R/W	1	Software Reset MAC core Driver set this bit to '0' to reset core of MAC. The reset duration is depended on whenever this bit is de-asserted by driver. There are only RXCURT and RXBOUND registers will be cleared by this bit. Others registers will not be affected 1 = in normal operation 0 = in reset status

4.23 MACID0--MAC ID0 Register

Offset Address = 0xFC70 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID15_0	R/W	0x0000	MAC ID Address [15:0]. This field defines lower address bit15 to bit0 of MAC. The MACID0, MACID1 and MACID2 combine into 48-bit MAC address. e.g. For the 48-bit MAC address 12-34-56-78-9A-BC, the driver should set MACID0=0x3412, MACID1=0x7856 and MACID2=0xBC9A. If the EEPROM is attached, this field will be auto-loaded from EEPROM after hardware reset.

4.24 MACID1--MAC ID1 Register

Offset Address = 0xFC74h Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID31_16	R/W	0x0000	MAC ID Address [31:16].

4.25 MACID2--MAC ID2 Register

Offset Address = 0xFC78 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID47_32	R/W	0x0000	MAC ID Address [47:32].

4.26 TXLEN--TX Length Register

Offset Address = 0xFC7C Default = 0x0000_05FC

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	MAXTXLEN	R/W	0x5FC	Max TX packet size This field defines the maximum raw packet size in transmittance for 10/100Mbps mode. It is not included 4 bytes CRC.

4.27 RXFILTER--RX Packet Filter Register

Offset Address = 0xFC80 Default = 0x0000_0004

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	GOODCRC	R/W	0	Good CRC enable When this bit is enabled, AX88180 will receive any packet of good CRC. 1 = enable 0 = disable
4	MULTI_HASH	R/W	0	Receive Multicast packet by *lookup hash table*. When this is enabled, AX88180 will receive multicast packet by the hash mapping function. It will refer to HASTAB0, HASHTAB1, HASHTAB2 and HASHTAB3 to look up the table. 1 = enable 0 = disable
3	BROADCAST	R/W	0	Receive Broadcast packet When this bit is enabled, AX88180 will receive the broadcast packet 1 = enable 0 = disable
2	UNICAST	R/W	1	Receive Directed Packet. If this bit is enabled, AX88180 will compare the destination address field of received packet with the address of MAC (refer to MACID0, MACID1, MACID2). When it is matched and good CRC, the packet will be passed to driver. Otherwise it will be dropped. 1 = enable 0 = disable
1	MULTICAST	R/W	0	Receive all Multicast Packets. If this bit is enabled, any multicast packet (good CRC) will be received and passed to driver. 1 = enable 0 = disable
0	RXANY	R/W	0	Receive Anything. If this bit is enabled, any packet whether it is good or fail will be received and passed to driver. 1 = enable 0 = disable

4.28 MDIOCTRL--MDIO Control Register

Offset Address = 0xFC84 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	WTEN	R/W	0	Write Enable. Driver enables this bit to issue a write cycle to PHY, it will be auto-cleared when AX88180 finishes the write cycle 1 = enable 0 = disable
14	RDEN	R/W	0	Read Enable. Driver enables this bit to issue a read cycle to PHY. This bit will be auto-cleared when AX88180 finishes the read cycle 1 = enable 0 = disable
12:8	PHYCRIDX	R/W	00000	PHY Register Index Driver sets this field to define the internal register index of PHY when it accesses PHY.
7:5	-	R	000	Reserved
4:0	PHYID	R/W	00000	PHY ID Driver sets the PHY ID value in this field. AX88180 will refer to this field when it accesses PHY by MDIO/MDC signals.

4.29 MDIODP--MDIO Data Port Register

Offset Address = 0xFC88 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	MDPORT	R/W	All 0's	PHY Data Port To or from PHY data is put in this field.

4.30 GPIO_CTRL--GPIO Control Register

Offset Address = 0xFC8C Default = 0x0000_0003

Field	Name	Type	Default	Description
31:10	-	R	All 0's	Reserved
9	GPIO1S	R/W	0	GPIO1 Status This bit stands for the pin status of GPIO1 when it is set to input mode. 1 = high state 0 = low state
8	GPIO0S	R/W	0	GPIO0 Status This bit stands for the pin status of GPIO0 when it is set to input mode. 1 = high state 0 = low state
7:2	-	R	All 0's	Reserved
1	GPIO1DIR	R/W	1	GPIO1 Mode Direction This field defines the direction of GPIO1 pin. 1 = input mode 0 = output mode
0	GPIO0DIR	R/W	1	GPIO0 Mode Direction This field defines the direction of GPIO pin. 1 = input mode 0 = output mode

Note: For output mode, software must firstly set the bit0 or bit1 to output mode then set bit8 or bit9.

4.31 RXINDICATOR--Receive Indicator Register

Offset Address= 0xFC90 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:1	-	R	All 0's	Reserved
0	RXSTART	R/W	0	Receive Start Driver sets this bit to start or end receive operation from RX buffer of AX88180. 1= Start read RX buffer 0= End read RX buffer

4.32 TXST--TX Status Register

Offset Address = 0xFC94 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:4	-	R	All 0's	Reserved
3	TXD3FAIL	R	0	TX Descriptor3 Transmit Fail When this bit is set 1, it means AX88180 fails in transmission of descriptor3. This bit will be self-cleared when driver reads TXST register.
2	TXD2FAIL	R	0	TX Descriptor2 Transmit Fail When this bit is set 1, it means A88180 fails in transmission of descriptor2. This bit will be self-cleared when driver reads TXST register.
1	TXD1FAIL	R	0	TX Descriptor1 Transmit Fail When this bit is set 1, it means AX88180 fails in transmission of descriptor1. This bit will be self-cleared when driver reads TXST register.
0	TXD0FAIL	R	0	TX Descriptor0 Transmit Fail When this bit is set 1, it means AX88180 fails in transmission of descriptor0. This bit will be self-cleared when driver reads TXST register.

4.33 MDCLKPAT--MDC Clock Pattern Register

Offset Address = 0xFCA0 Default = 0x0000_8040

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:8	-	R/W	0x80	Reserved, must set to 0x80 for normal operation
7:0	MDCPAT	R/W	0x40	MDC Clock Divide Factor This field defines the divided factor of host clock. AX88180 will refer to this field and generate a low speed clock to PHY.

4.34 RXCHKSUMCNT--RX IP/UDP/TCP Checksum Error Counter

Offset Address = 0xFCA4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	RXCHKERCNT	R/W	All 0's	RX Checksum Error Counter If the RXCHKSUM field of RX_CFG register is set to '1', MAC will check the checksum of IP, TCP or UDP packet. Whenever there is checksum error detected, this field will be added one. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.35 RXCRCNT--RX CRC Error Counter

Offset Address = 0xFCA8 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	RXCRCCNT	R/W	All 0's	RX CRC32 Error Counter MAC checks the received packet. If there is a CRC error detect, this field will be added one. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.36 TXFAILCNT--TX Fail Counter

Offset Address = 0xFCAC Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	TXFILCNT	R/W	All 0's	TX Fail Counter This field records the number of transmitted error for TX packet. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.37 PROMDPR--EEPROM Data Port Register

Offset Address = 0xFCB0 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	PROMDP	R/W	All 0's	EEPROM Data Port The data to or from EEPROM is set in this field.

4.38 PROMCTRL--EEPROM Control Register

Offset Address= 0xFCB4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:15	-	R	All 0's	Reserved
14:12	ROM_CMD	R/W	000	EEPROM Command Code. Driver set this field to represent what type command will be send to EEPROM device. 110 = read command 111 = erase command 101 = write command
11	ROM_WT	R/W	0	Write EEPROM Set to '1' to write EEPROM, it will be auto-cleared when AX88180 finishes the write operation.
10	ROM_RD	R/W	0	Read EEPROM Set to '1' to read EEPROM, it will be cleared when MAC finished the read operation. Driver can read PROMDPR register to get the returned data.
9	ROM_RLD	R/W	0	Reload EEPROM Set to '1' to re-load EEPROM, this bit will be auto-cleared when AX88180 finishes loading operation.
8	-	R	0	Reserved
7:0	ROM_ADDR	R/W	0x00	EEPROM Address Set this field to define the address for serial EEPROM access. (only support 16-bit data access, e.g. 93C56 type)

4.39 MAXRXLEN--Max. RX Packet Length Register

Offset Address= 0xFCB8 Default = 0x0000_0600

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXLEN	R/W	0x600	Max RX Packet length This field defines the max length of received packet. It doesn't include 4-byte CRC.

4.40 HASHTAB0--Hash Table0 Register

Offset Address = 0xFCC0 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB0	R/W	0x0000	Hash table: bit15~bit0 Driver sets HASHTAB0, HASHTAB1, HASHTAB2 and HASHTAB3 to define 64-bit hash table. AX88180 will refer this table to check multicast packet if multicast filter is enabled (bit4 of RXFILTER) for RX. When AX88180 receives a packet then it extracts the destination address (DA). The DA is calculated by CRC32 algorithm. After the operation, AX88180 will grab the MSB[31:27] of result as hash table index. The range of index is from 0 to 63. For example, the hash table is composite as {HASHTAB3[15:0], HASHTAB2[15:0], HASHTAB1[15:0], HASHTAB0[15:0]}. If AX88180 detects the MSB[31:27] = 26 of CRC32 of DA for someone multicast packet, and driver set '1' to HASHTAB1[10], then the multicast packet will received by AX88180.

4.41 HASHTAB1--Hash Table1 Register

Offset Address = 0xFCC4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB1	R/W	0x0000	Hash table: bit31~bit16

4.42 HASHTAB2--Hash Table2 Register

Offset Address = 0xFCC8 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB2	R/W	0x0000	Hash table: bit47~bit32

4.43 HASHTAB3--Hash Table3 Register

Offset Address = 0xFCCC Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB3	R/W	0x0000	Hash table: bit63 ~ bit48

4.44 DOGTHD0—Watch Dog Timer Threshold0 Register

Offset Address = 0xFCE0 Default = 0x0000_FFFF

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	DOGTH0	R/W	0xFFFF	Watch Dog Timer Low Word This register and DOGTHD1[11:0] are defined to an expired threshold for internal watchdog counter. The threshold {[DOGTHD1, DOGTHD0] is a 28-bit value. To multiply 28-bit value with one-cycle period of a host clock is the expired duration. If the DOGEN is set to '1' and WDTEI of ISR is set, then AX88180 will periodically generate interrupt whenever the counter reaches to the threshold.

4.45 DOGTHD1—Watch Dog Timer Threshold1 Register

Address = 0xFCE4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	DOGEN	R/W	0	Dog Timer Enable 1 = Enable internal dog timer 0 = Disable
14:12	-	R/W	All 0's	Reserved
11:0	DOGTH1	R/W	0x000	Dog Timer High Field. This field and DOGTHD0[15:0] combine to a 28-bit register.

4.46 SOFTRST --- Software Reset Register

Address = 0xFCEC Default = 0x0000_0003

Field	Name	Type	Default	Description
31:2	-	R	All 0's	Reserved
1	-	R/W	1	Reserved
0	RST_MAC	R/W	1	Software Reset enable Driver set this bit to '0' to reset MAC. The reset duration is depended on whenever this bit is de-asserted by driver. Most registers will be cleared to default value. 1 = in normal operation 0 = in reset status

5.0 Electrical Specification and Timings

5.1 DC Characteristics

5.1.1 Absolute Maximum Ratings

Symbol	Description	Rating	Units
T_{STG}	Storage Temperature	-40 to 150	°C
VCC3	Power supply of 3.3V	-0.3 to VCC3 + 0.3	V
VCC2	Power supply of 2.5V	-0.3 to VCC2 + 0.3	V
V_{I3}	Input voltage of 3.3V IO with 5V tolerance	-0.3 to 5.5	V
V_{I2}	Input voltage of 2.5V IO with 3.3V tolerance	-0.3 to 3.9	V

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.

5.1.2 General Operation Conditions

Symbol	Description	Min	Typ	Max	Units
Tj	Junction temperature	0	-	115	°C
VCC2	Supply Voltage of 2.5V	2.25	2.5	2.75	V
VCC3	Supply Voltage of 3.3V	3.0	3.3	3.6	V
V_{I3}	Input voltage of 3.3V IO with 5V tolerance	0	3.3	5.25	V
V_{I2}	Input voltage of 2.5V IO with 3.3V tolerance	0	2.5	3.6	V

5.1.3 Leakage Current and Capacitance

Symbol	Description	Min	Typ	Max	Units
I_{IN}	Input Leakage Current	-10	±1	+10	µA
I_{OZ}	Tri-state leakage current	-10	±1	+10	µA
C_{OUT}	Output capacitance	-	3.1	-	pF
C_{BID}	Bi-directional buffer capacitance	-	3.1	-	pF

5.1.4 DC Characteristics of 2.5V IO Pins

Symbol	Description	Min	Typ	Max	Units
VCC2	Power supply of 2.5V IO	2.25	2.5	2.75	V
Vil	Input low voltage	-	-	0.7	V
Vih	Input high voltage	1.7	-	-	V
Vol	Output low voltage	-	-	0.4	V
Voh	Output high voltage	1.85			V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ

5.1.5 DC Characteristics of 3.3V IO Pins

Symbol	Description	Min	Typ	Max	Units
VCC3	Power supply of 3.3V IO	3.0	3.3	3.6	V
Vil	Input low voltage	-	-	0.8	V
Vih	Input high voltage	2.0	-	-	V
Vol	Output low voltage	-	-	0.4	V
Voh	Output high voltage	2.4			V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ

5.2 Thermal Characteristics

A. Junction to ambient thermal resistance, θ_{JA}

Symbol	Min	Typ	Max	Units
θ_{JA}	-	46.3	-	°C/W

B. Junction to case thermal resistance, θ_{JC}

Symbol	Min	Typ	Max	Units
θ_{JC}	-	16.2		°C/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P}, \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature
T_A: ambient or environment temperature
T_C: the top center of compound surface temperature
P: input power (watts)

5.3 Power Consumption

Device Only

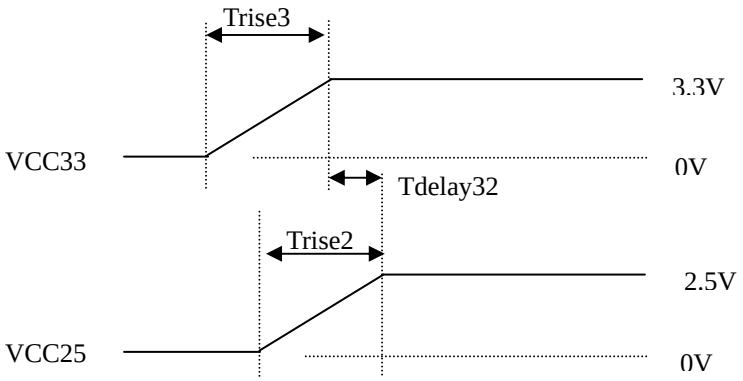
Measurement bases on 100MHz frequency of HCLK and turn on internal regulator at 25 °C temperature.

Item	Symbol	Power-on with cable removed	Operation at 10Base-T	Operation at 100Base-T	Operation at 1000Base-T	Stand-by current (HCLK is off)	Units
1	VCC3 (IO)	1.6	1.8	2.4	2.5	0.061	mA
2	VCC3R	87	72	79	105	1.5	mA

Note: The current of VCC3R includes VCC2 core current.

5.4 Power-up sequence

At power-up, AX88180 requires the VCC33 power supply to rise to normal operating voltage within Trise3 and the VCC25 power supply to rise to nominal operating voltage within Trise2.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	-	-	10	ms
T_{rise2}	2.5V power supply rise time	From 0V to 2.5V	-	-	10	ms
$T_{delay32}$	3.3V rise to 2.5V rise time delay		-5	-	5	ms

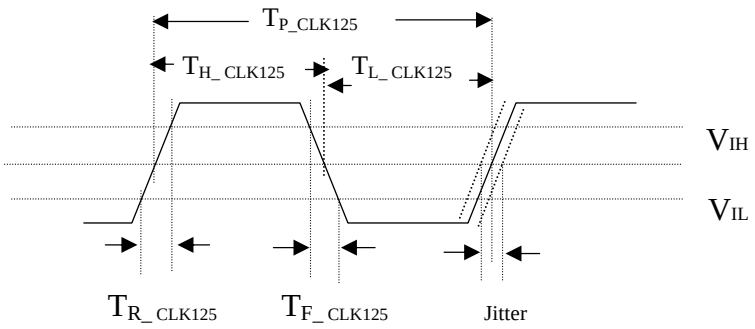
5.5 A.C. Timing Characteristics

5.5.1 Host Clock

A. Reference clock (HCLK)

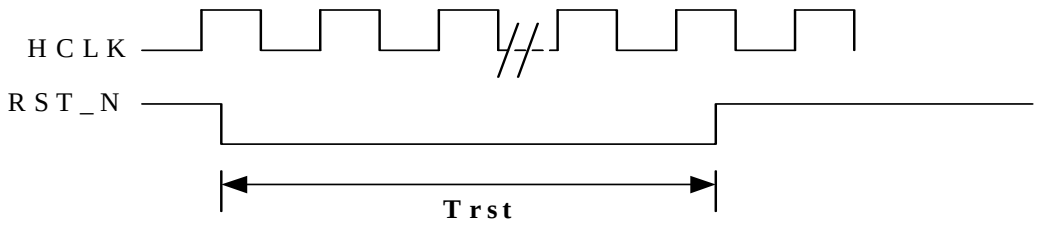
Description	Min	Typ.	Max	Units
Reference frequency	40	-	100	MHz
Reference clock duty cycle	40	50	60	%

B. Reference clock (CLK125)



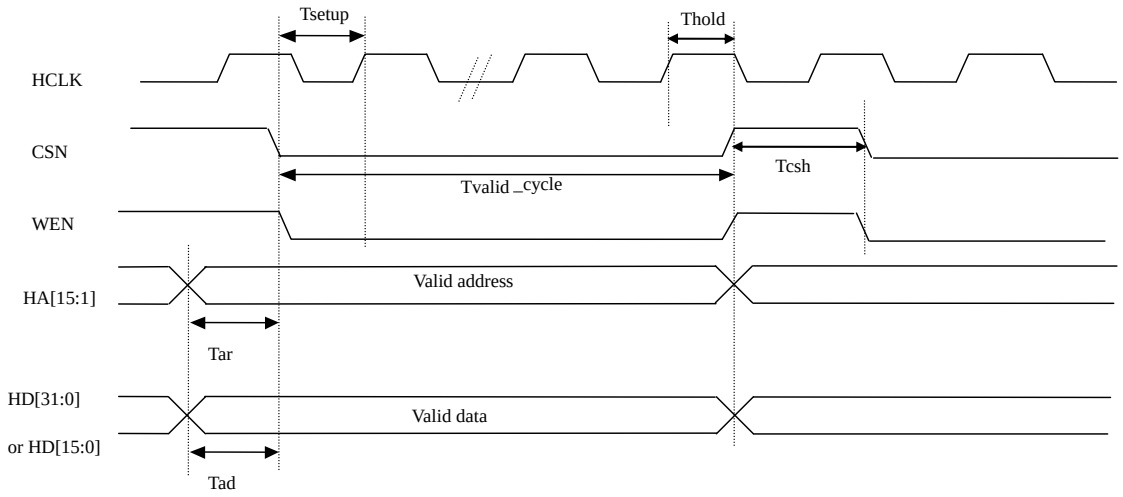
Symbol	Parameter	Condition	Min	Typ	Max	Unit
-	Frequency			125		MHz
T_{P_CLK125}	CLK125 clock cycle time		7.5	8.0	8.5	ns
T_{H_CLK125}	CLK125 clock high time		2.5	4.0	-	ns
T_{L_CLK125}	CLK125 clock low time		2.5	4.0	-	ns
T_{R_CLK125}	CLK125 rise time	V_{IL} (max) to V_{IH} (min)	-	-	1.0	ns
T_{F_CLK125}	CLK125 fall time	V_{IH} (min) to V_{IL} (max)	-	-	1.0	ns
	CLK125 Jitter		-100	-	+100	ps

5.5.2 Reset Timing



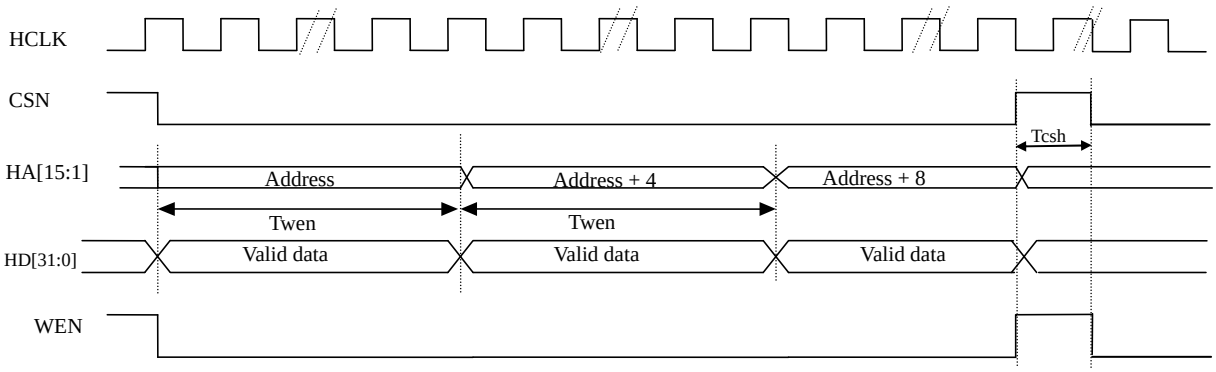
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	0.5	-	-	ms

5.5.3 Host Single Write Timing



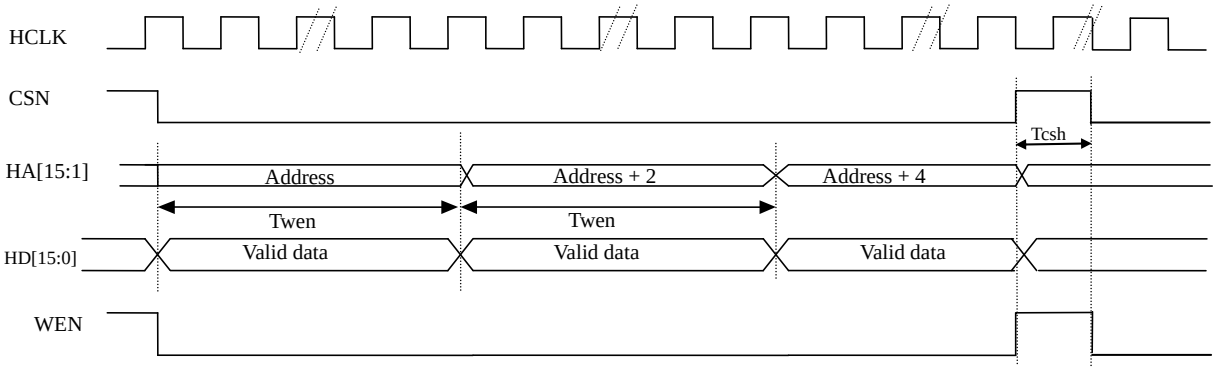
Symbol	Description	Min	Typ.	Max	Units
Tsetup	CSN, WEN, HA, HD to HCLK setup timing (synchronous to MCU)	0	-	-	ns
Tsetup	CSN, WEN, HA, HD to HCLK setup timing (asynchronous to MCU)	-	-	-	ns
Thold	CSN, WEN, HA, HD to HCLK hold timing (synchronous to MCU)	2.5	-	-	ns
Thold	CSN, WEN, HA, HD to HCLK hold timing (asynchronous to MCU)	-	-	-	ns
Tar	HA exceed to WEN timing	0	-	-	HCLK
Tad	HA exceed to WEN timing	0	-	-	HCLK
Tvalid_cycle	A Valid write cycle timing (synchronous to MCU)	5	-	-	HCLK
Tvalid_cycle	A Valid write cycle timing (asynchronous to MCU)	6	-	-	HCLK
Tcsh	CSN, WEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, WEN Deassertion time (asynchronous to MCU)	1.5			HCLK

5.5.4 Host Burst Write Timing (32-bit mode)



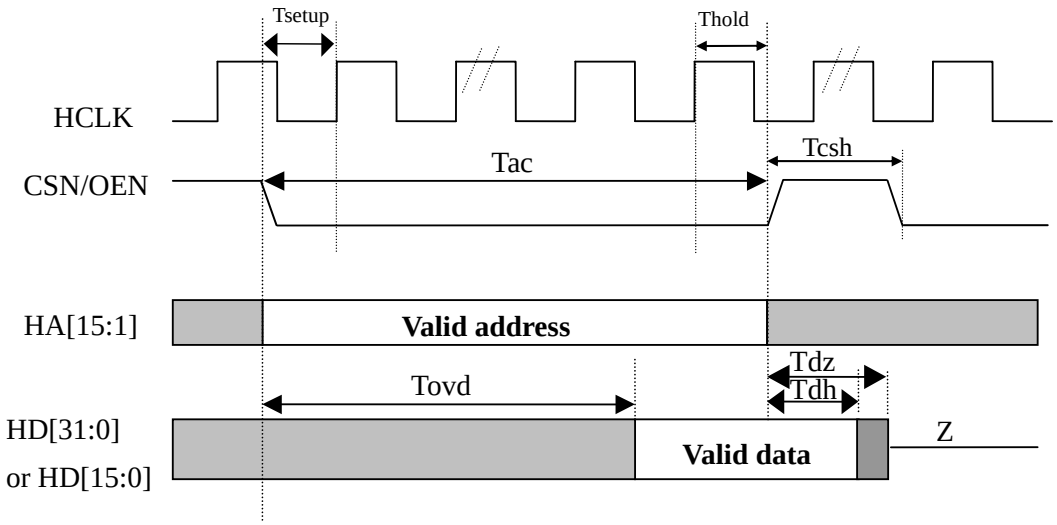
Symbol	Description	Min	Typ.	Max	Units
Twen	Valid write cycle timing (synchronous to MCU)	5	-	-	HCLK
Twen	Valid write cycle timing (asynchronous to MCU)	6	-	-	HCLK
Tcsh	CSN, WEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, WEN Deassertion time (asynchronous to MCU)	1.5			HCLK

5.5.5 Host Burst Write Timing (16-bit mode)



Symbol	Description	Min	Typ.	Max	Units
Twen	Valid write cycle timing (synchronous to MCU)	5	-	-	HCLK
Twen	Valid write cycle timing (asynchronous to MCU)	6	-	-	HCLK
Tcsh	CSN, WEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, WEN Deassertion time (asynchronous to MCU)	1.5			HCLK

5.5.6 Host Single Read Timing



Symbol	Description	Min	Typ.	Max	Units
Tsetup	CSN, OEN, HA to HCLK setup timing (synchronous to MCU)	0	-	-	ns
Tsetup	CSN, OEN, HA to HCLK setup timing (asynchronous to MCU)	-	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (synchronous to MCU)	2.5	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (asynchronous to MCU)	-	-	-	ns
Tac	CSN/OEN access timing (synchronous to MCU)	*1	-	-	HCLK
Tac	CSN/OEN access timing (asynchronous to MCU)	*2	-	-	HCLK
Tovd	OEN assert to valid data timing (synchronous to MCU)	-	-	3xHCLK +14 ns *3	HCLK
Tovd	OEN assert to valid data timing (asynchronous to MCU)	-	-	4xHCLK +14 ns *3	HCLK
Tcsh	CSN, OEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, OEN Deassertion time (asynchronous to MCU)	1.5			HCLK
Tdh	Valid data hold timing to OEN de-asserted	0	-	-	ns
Tdz	Data buffer turn off time	-	-	7	ns

*1 : synchronous mode Tac is derived from synchronous mode Tovd.

If HCLK=100Mhz, Tovd = 3x10ns+14ns=44ns. The minimum Tac will be 5 cycles of HCLK.

If HCLK=50Mhz, Tovd = 3x20ns+14ns =74ns. The minimum Tac will be 4 cycles of HCLK.

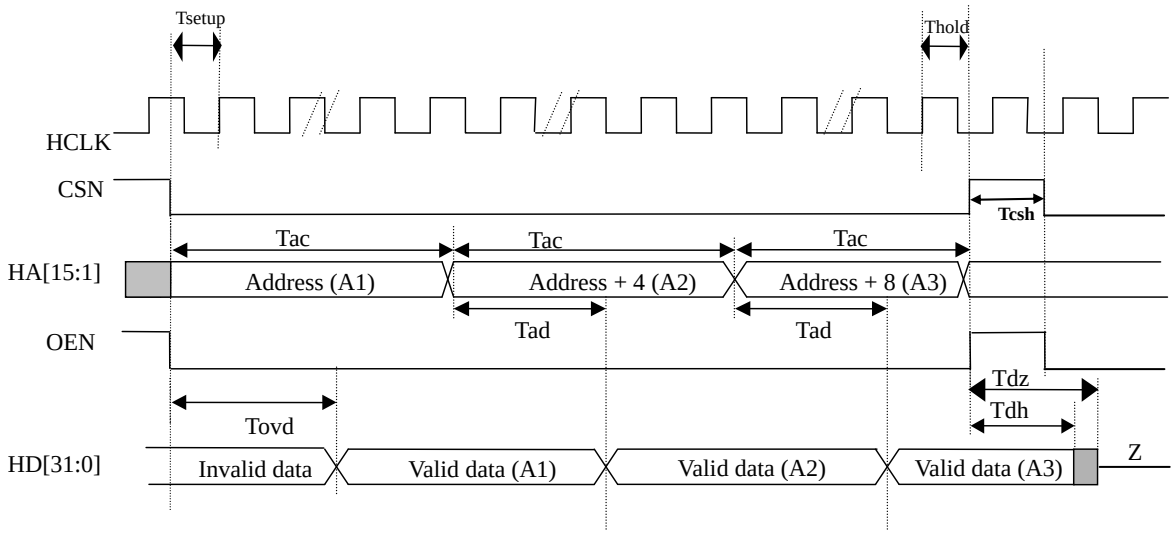
*2 : asynchronous mode Tac is derived from asynchronous mode Tovd.

If HCLK=100Mhz, Tovd = 4x10ns+14ns=54ns. The minimum Tac will be 6 cycles of HCLK.

If HCLK=50Mhz, Tovd = 4x20ns+14ns =94ns. The minimum Tac will be 5 cycles of HCLK.

*3 : Test load 40pF on HD[31:0] or HD[15:0].

5.5.7 Host Burst Read Timing (32-bit mode)



Symbol	Description	Min	Typ.	Max	Units
Tsetup	CSN, OEN, HA to HCLK setup timing (synchronous to MCU)	0	-	-	ns
Tsetup	CSN, OEN, HA to HCLK setup timing (asynchronous to MCU)	-	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (synchronous to MCU)	2.5	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (asynchronous to MCU)	-	-	-	ns
Tac	Valid address access timing (synchronous to MCU)	*1	-	-	HCLK
Tac	Valid address access timing (asynchronous to MCU)	*2	-	-	HCLK
Tovd	OEN assert to valid data timing (synchronous to MCU)	-	-	3xHCLK +14 ns *3	HCLK
Tovd	OEN assert to valid data timing (asynchronous to MCU)	-	-	4xHCLK +14 ns *3	HCLK
Tad	Burst mode address to valid data (synchronous to MCU)	-	-	3xHCLK +14 ns *3	HCLK
Tad	Burst mode address to valid data (asynchronous to MCU)	-	-	4xHCLK +14 ns *3	HCLK
Tcsh	CSN, OEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, OEN Deassertion time (asynchronous to MCU)	1.5			HCLK
Tdh	Valid data hold timing to OEN de-asserted	0	-	-	ns
Tdz	Data buffer turn off time	-	-	7	ns

*1 : synchronous mode Tac is derived from synchronous mode Tovd, Tad

If HCLK=100Mhz, Tovd = 3x10ns +14ns=44ns. The minimum Tac will be 5 cycles of HCLK.

If HCLK=50Mhz, Tovd = 3x20ns +14ns =74ns. The minimum Tac will be 4 cycles of HCLK.

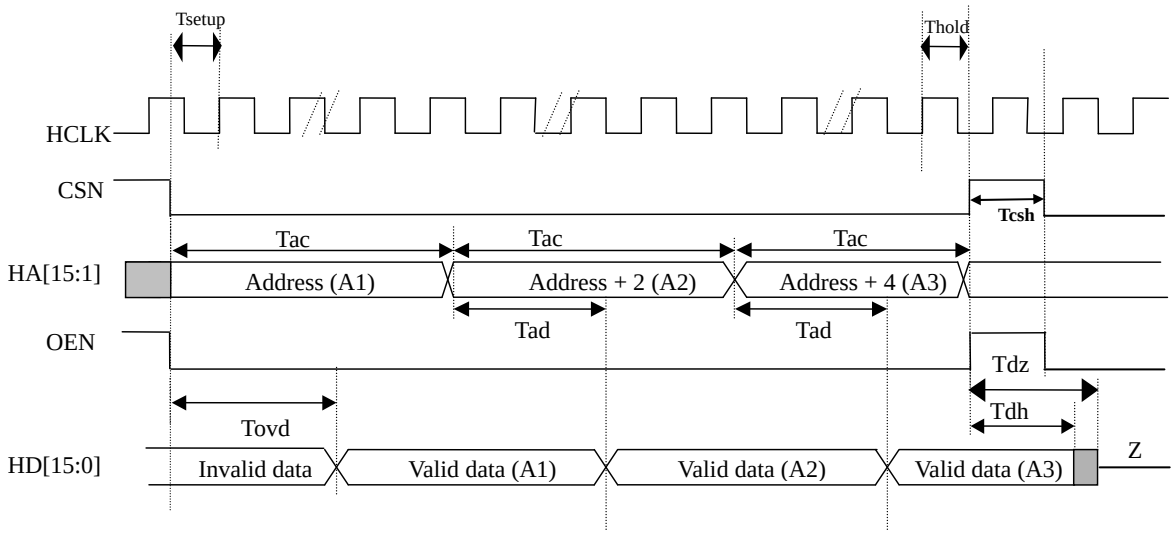
*2 : asynchronous mode Tac is derived from asynchronous mode Tovd, Tad

If HCLK=100Mhz, Tovd = 4x10ns +14ns=54ns. The minimum Tac will be 6 cycles of HCLK.

If HCLK=50Mhz, Tovd = 4x20ns +14ns =94ns. The minimum Tac will be 5 cycles of HCLK.

*3 : Test load 40pF on HD[31:0].

5.5.8 Host Burst Read Timing (16-bit mode)



Symbol	Description	Min	Typ.	Max	Units
Tsetup	CSN, OEN, HA to HCLK setup timing (synchronous to MCU)	0	-	-	ns
Tsetup	CSN, OEN, HA to HCLK setup timing (asynchronous to MCU)	-	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (synchronous to MCU)	2.5	-	-	ns
Thold	CSN, OEN, HA to HCLK hold timing (asynchronous to MCU)	-	-	-	ns
Tac	Valid address access timing (synchronous to MCU)	*1	-	-	HCLK
Tac	Valid address access timing (asynchronous to MCU)	*2	-	-	HCLK
Tovd	OEN assert to valid data timing (synchronous to MCU)	-	-	3xHCLK +14 ns *3	HCLK
Tovd	OEN assert to valid data timing (asynchronous to MCU)	-	-	4xHCLK +14 ns *3	HCLK
Tad	Burst mode address to valid data (synchronous to MCU)	-	-	3xHCLK +14 ns *3	HCLK
Tad	Burst mode address to valid data (asynchronous to MCU)	-	-	4xHCLK +14 ns *3	HCLK
Tcsh	CSN, OEN Deassertion time (synchronous to MCU)	1			HCLK
Tcsh	CSN, OEN Deassertion time (asynchronous to MCU)	1.5			HCLK
Tdh	Valid data hold timing to OEN de-asserted	0	-	-	ns
Tdz	Data buffer turn off time	-	-	7	ns

*1 : synchronous mode Tac is derived from synchronous mode Tovd, Tad

If HCLK=100Mhz, Tovd = 3x10ns +14ns=44ns. The minimum Tac will be 5 cycles of HCLK.

If HCLK=50Mhz, Tovd = 3x20ns +14ns =74ns. The minimum Tac will be 4 cycles of HCLK.

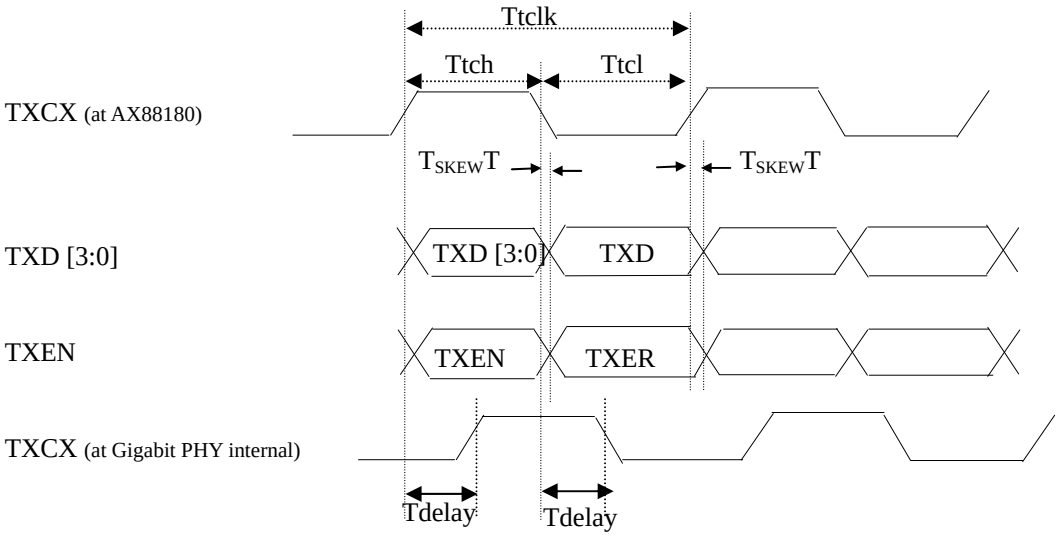
*2 : asynchronous mode Tac is derived from asynchronous mode Tovd, Tad

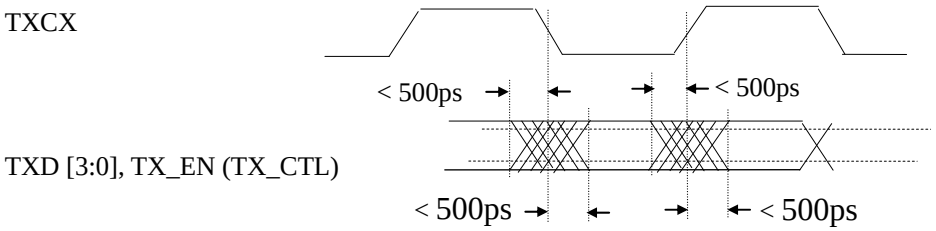
If HCLK=100Mhz, Tovd = 4x10ns +14ns=54ns. The minimum Tac will be 6 cycles of HCLK.

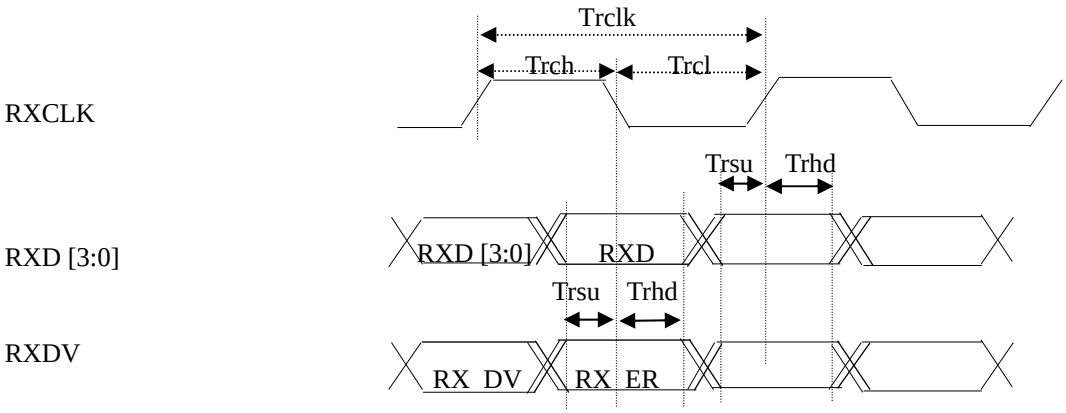
If HCLK=50Mhz, Tovd = 4x20ns +14ns =94ns. The minimum Tac will be 5 cycles of HCLK.

*3 : Test load 40pF on HD[15:0].

5.5.9 RGMII Timing







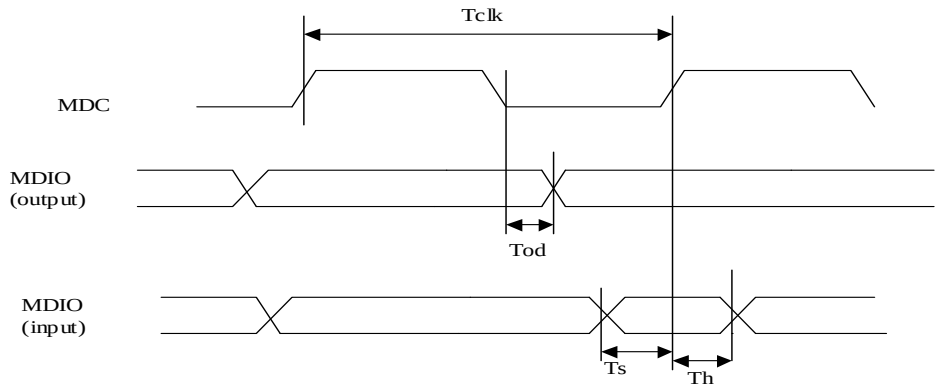
Symbol	Description	Min	Typ	Max	Units
Ttclk	TXCX clock cycle time at 1000Mbps *1	7.2	8.0	8.8	ns
Ttch	TXCX clock high time at 1000Mbps *2	-	4.0	-	ns
Ttcl	TXCX clock low time at 1000Mbps *2	-	4.0	-	ns
$T_{SKEW}T$	TXCX clock to TXD [3:0] and TXEN output skew (at transmitter)	-500	-	500	ps
Tdelay	Data to clock in Gigabit PHY internal delay *3	1.5	-	2.0	ns
Trclk	RXCLK clock cycle time at 1000Mbps *1	7.2	8.0	8.8	ns
Trch	RXCLK clock high time at 1000Mbps *2	-	4.0	-	ns
Trcl	RXCLK clock low time at 1000Mbps *2	-	4.0	-	ns
Trsu	RXD [3:0] and RXDV to RXCLK clock setup time	1.0	-	-	ns
Trhd	RXD [3:0] and RXDV to RXCLK clock hold time	1.0	-	-	ns

*1: For 10Mbps and 100Mbps, Ttclk and Trclk shall scale to 400ns+/-40ns and 40ns+/-4ns respectively.

*2: For 10Mbps and 100Mbps, the typical value of Ttch, Ttcl, Trch, and Trcl shall scale to 200ns and 20ns respectively.

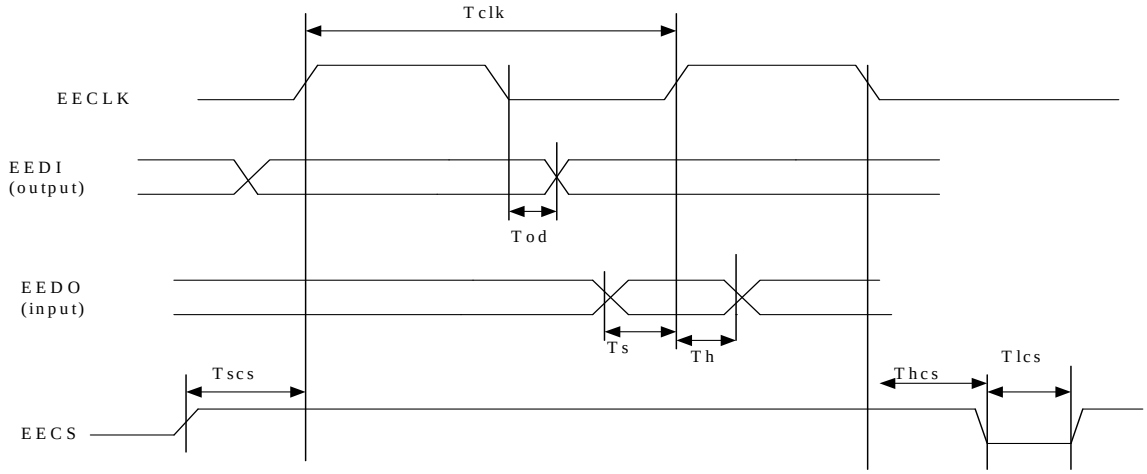
*3: The external Gigabit PHY needs to add a delay on the TXCX signal.

5.5.10 MDIO Timing



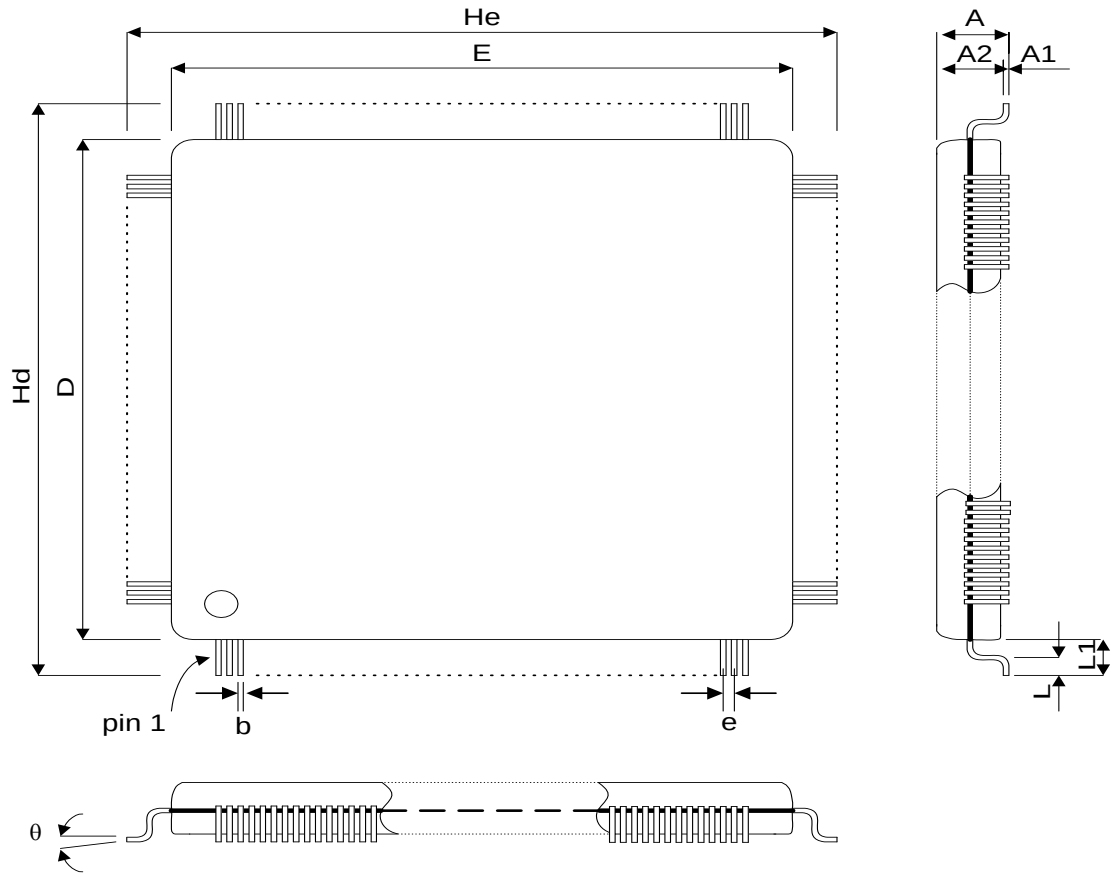
Symbol	Description	Min	Typ.	Max	Units
Tclk	MDC clock timing*		1340	-	ns
Tod	MDC falling edge to MDIO output delay		-	32	ns
Ts	MDIO data input setup timing	10	-	-	ns
Th	MDIO data input hold timing	4	-	-	ns

5.5.11 Serial EEPROM Timing



Symbol	Description	Min	Typ.	Max	Units
Tclk	EECLK clock timing*		1370	-	ns
Tod	EECLK falling edge to EEDI output delay		-	5	ns
Ts	EEDO data input setup timing	6	-	-	ns
Th	EEDO data input hold timing	6	-	-	ns
Tscs	EECS output valid to EECLK rising edge	650			ns
Thcs	EECLK falling edge to EECS invalid timing	0			ns
Tlcs	Minimum EECS low timing	-	560	-	ns

6.0 Package Information



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.1	
A2	1.35	1.4	1.45
A			1.6
b	0.13	0.18	0.23
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e		0.40	
Hd	15.85	16.00	16.15
He	15.85	16.00	16.15
L	0.45	0.60	0.75
L1		1.00	
θ	0		7

7.0 Ordering Information

AX88180	L	F
Product name	Package LQFP	F: Lead Free

Appendix A1. 16-bit Mode Host Interface Reference Connection

Note: The name of control signals for MCU is demonstrated only.

A1-1. 16-bit Synchronous Mode

Please refer to Appendix A3 for more details of system design considerations.

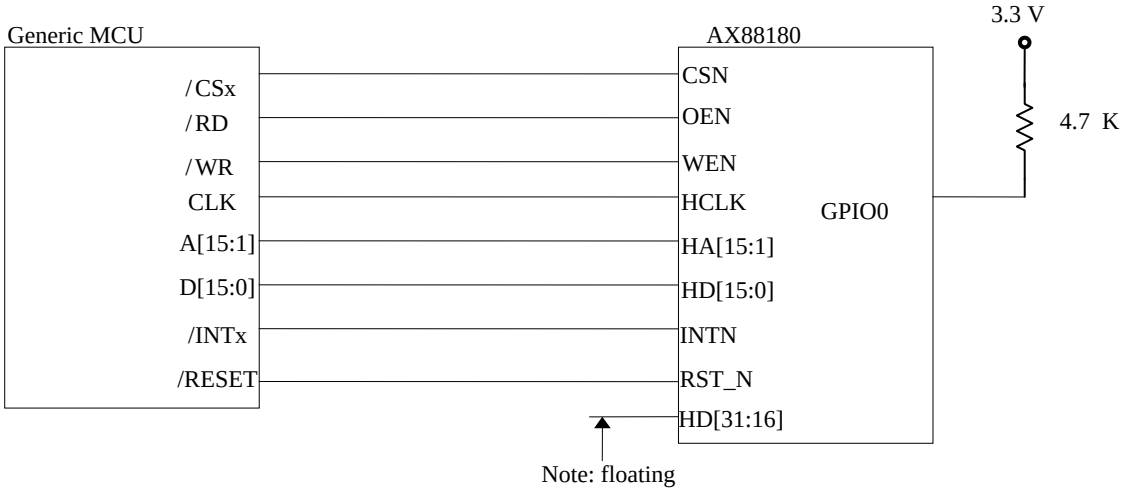


Figure 6. 16-bit Synchronous Mode Host I/F Connection with Synchronous Reset

A1-2. 16-bit Asynchronous Mode

The external OSC reference clocks should be synchronously provided to AX88180 HCLK while powering ON the system.

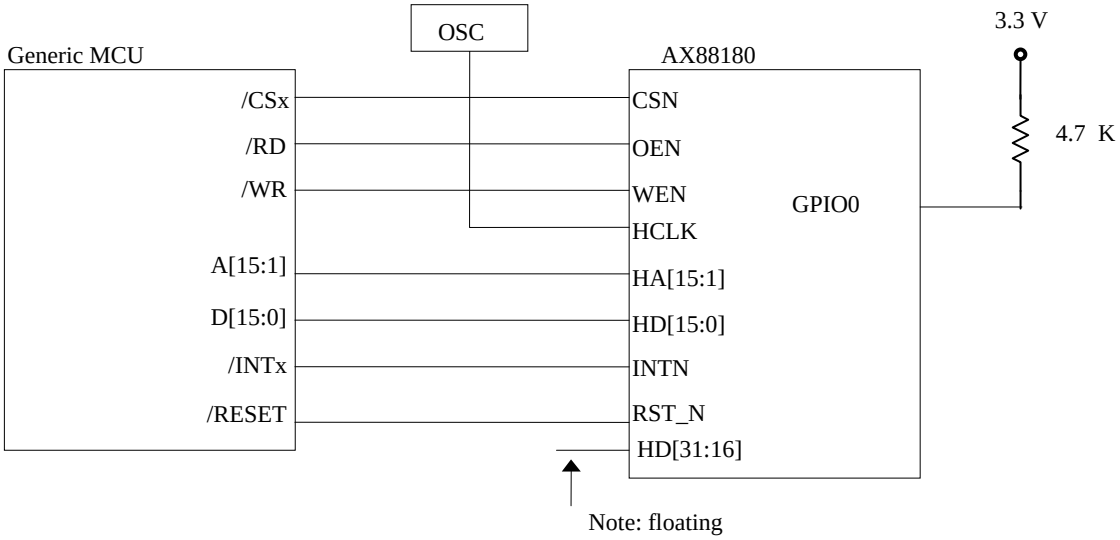


Figure 7. 16-bit Asynchronous Mode Host I/F Connection

Appendix A2. 32-bit Mode Host Interface Reference Connection

Note: The name of control signal for MCU is demonstrated only.

A2-1. 32-bit Synchronous Mode for Byte Alignment Address Mode MCU

Please refer to Appendix A3 for more details of system design considerations.

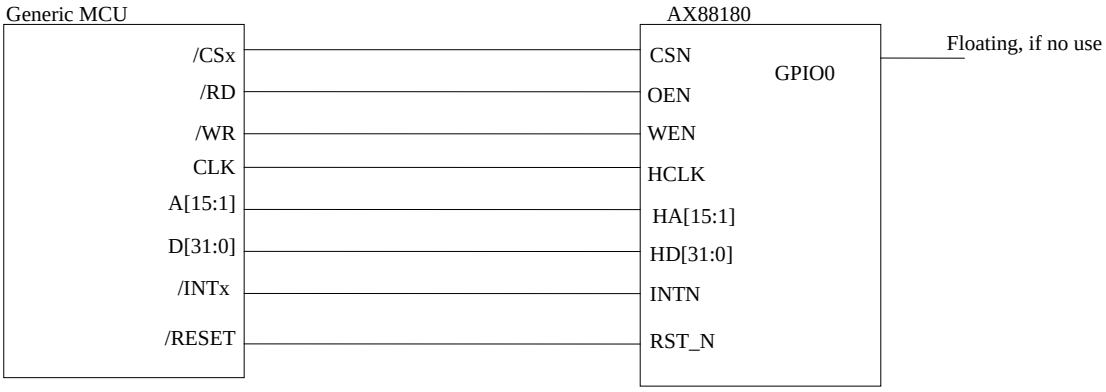


Figure 8. 32-bit Synchronous Mode Host I/F Connection with Synchronous Reset (for Byte-Aligned MCU)

A2-2. 32-bit Asynchronous Mode for Byte Alignment Address Mode MCU

The external OSC reference clocks should be synchronously provided to AX88180 HCLK while powering ON the system.

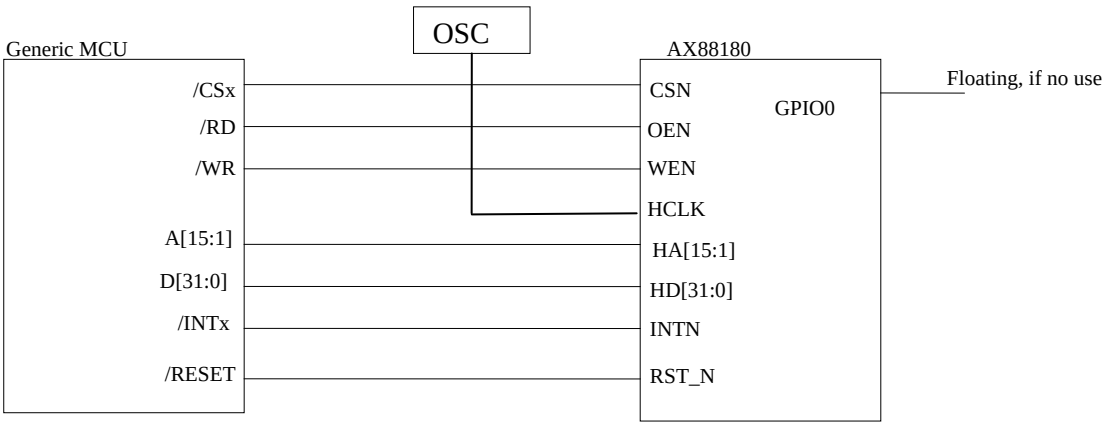


Figure 9. 32-bit Asynchronous Mode Host I/F Connection (for Byte-Aligned MCU)

A2-3. 32-bit Synchronous Mode for Double-Word Alignment Address Mode MCU

Please refer to Appendix A3 for more details of system design considerations.

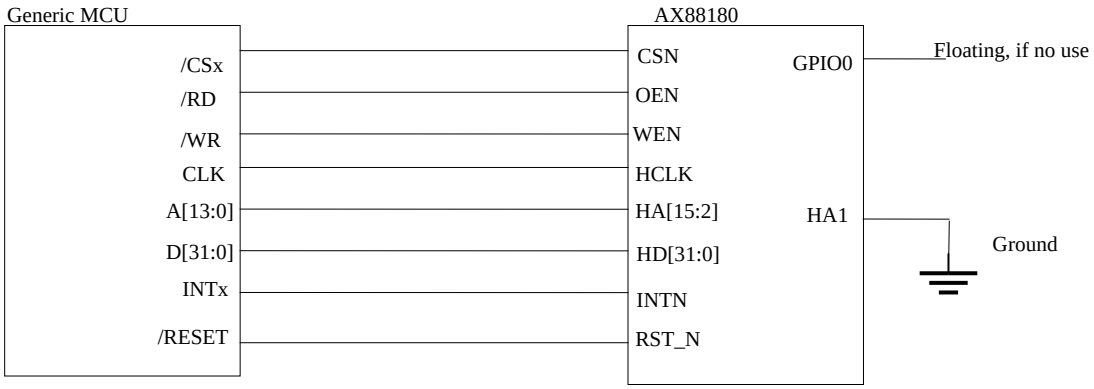


Figure 10. 32-bit Synchronous Mode Host I/F Connection with Synchronous Reset (for DWORD-Aligned MCU)

A2-4. 32-bit Asynchronous Mode for Double-Word Alignment Address Mode MCU

The external OSC reference clocks should be synchronously provided to AX88180 HCLK while powering ON the system.

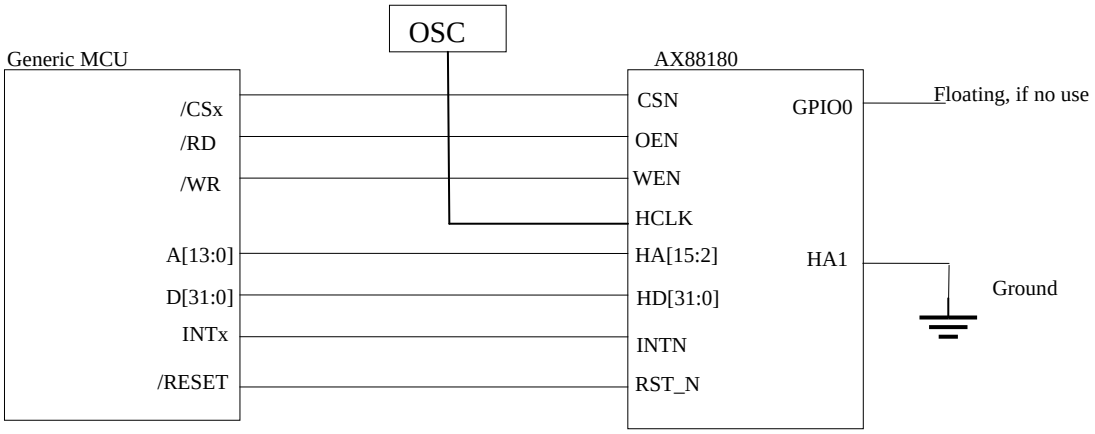


Figure 11. 32-bit Asynchronous Mode Host I/F Connection (for DWORD-Aligned MCU)

Appendix A3. System Power Up Reference Clock Design Considerations

The AX88180 HCLK clock signals MUST be provided synchronously for AX88180 synchronous reset and hardware configuration during booting up the system at AX88180 synchronous mode.

The MCU might not be able to synchronously provide the clock signals to AX88180 HCLK while powering ON the system. In this case, an addition OR logic gate is necessary between MCU's /RD signal and AX88180's OEN signal to avoid bus contention on HD bus. And the isolate control signal of the OR logic gate can be the /CSx signal which from MCU.

The following is an example of the host interface reference connection between AX88180 and MCU when the MCU can't synchronously provide the clock signals to AX88180 HCLK while powering ON the system.

Note that the data accessing time of MCU should consider both the AX88180 data access timing and the OR gate delay time. The delay time (T_{delay}) of the OR gate should be as short as possible.

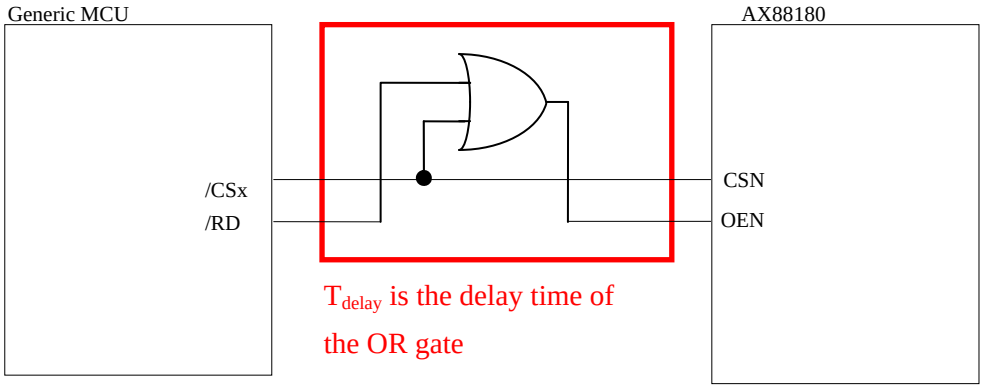


Figure 12. An Example of Host I/F Connection with OR Logic Gate Circuit

The following is an example of host data accessing timing with OR logic gate circuit (e.g. with 10ns delay time).

(1) For synchronous mode, Tac_delay is derived from synchronous mode Tovd and Tdelay,
If HCLK=100Mhz, Tovd (3 HCLK + 14ns) = 3x10ns +14ns=44ns and Tdelay = 10ns, the minimum Tac_delay will be 6 cycles of HCLK.
If HCLK=50Mhz, Tovd (3 HCLK + 14ns) = 3x20ns +14ns =74ns and Tdelay = 10ns, the minimum Tac_delay will be 5 cycles of HCLK.

(2) For asynchronous mode, Tac_delay is derived from synchronous mode Tovd and Tdelay,
If HCLK=100Mhz, Tovd (4 HCLK + 14ns) = 4x10ns +14ns=54ns and Tdelay = 10ns, the minimum Tac_delay will be 7 cycles of HCLK.
If HCLK=50Mhz, Tovd (4 HCLK + 14ns) = 4x20ns +14ns =94ns and Tdelay = 10ns, the minimum Tac_delay will be 6 cycles of HCLK.

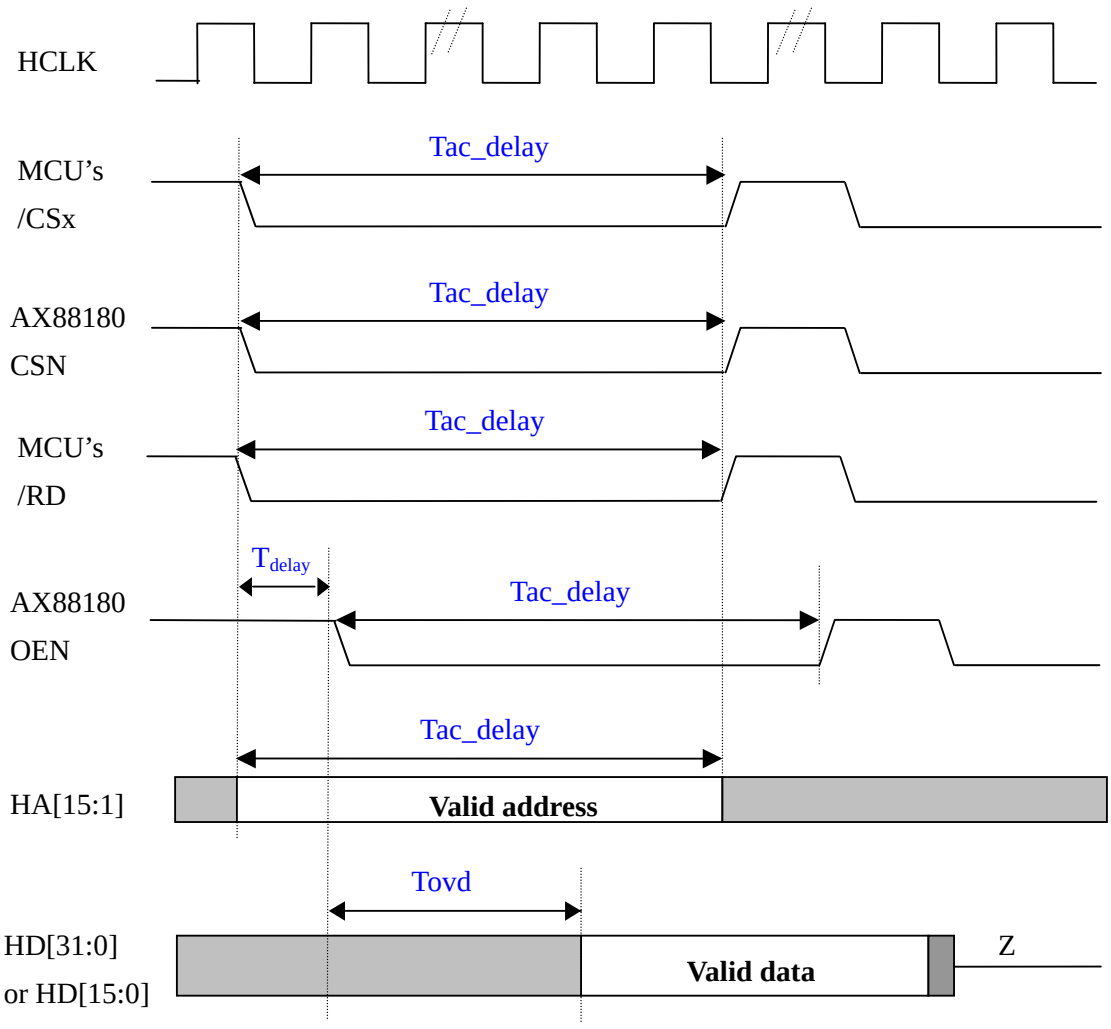


Figure 13. An Example of Host Data Accessing Timing with OR Logic Gate Circuit

Appendix A4. RGMII/MII Interface Reference Connection

A4-1. RGMII Interface Reference Connection

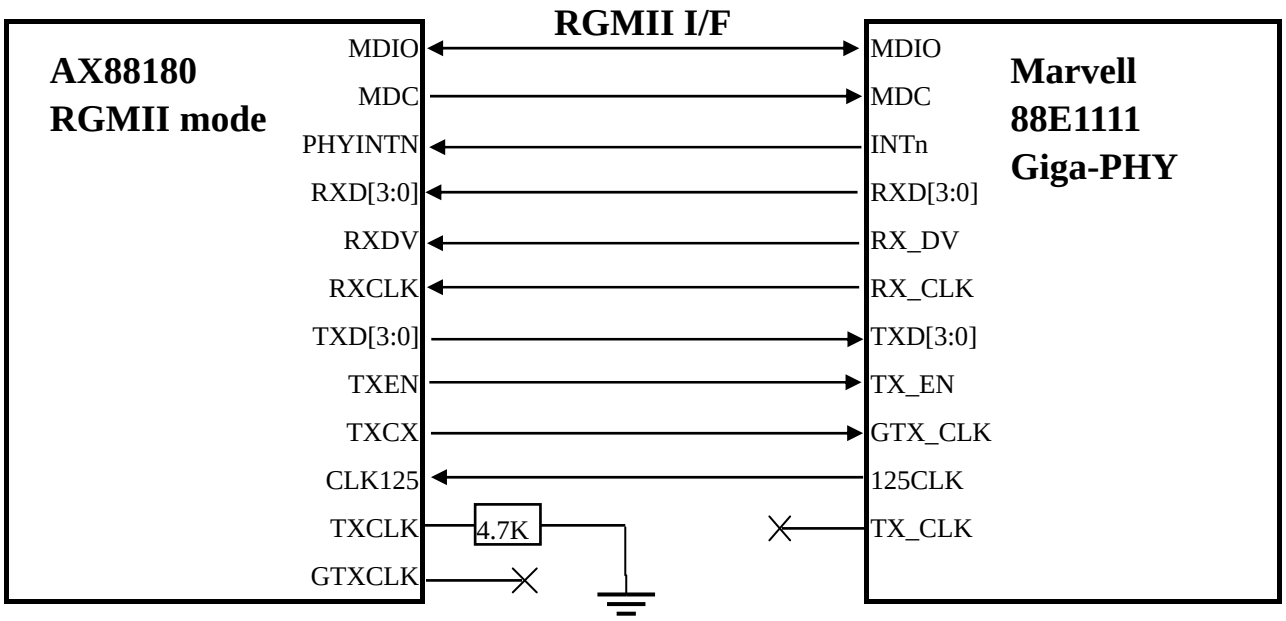


Figure 14. RGMII Interface Reference Connection

A4-2. MII Interface Reference Connection

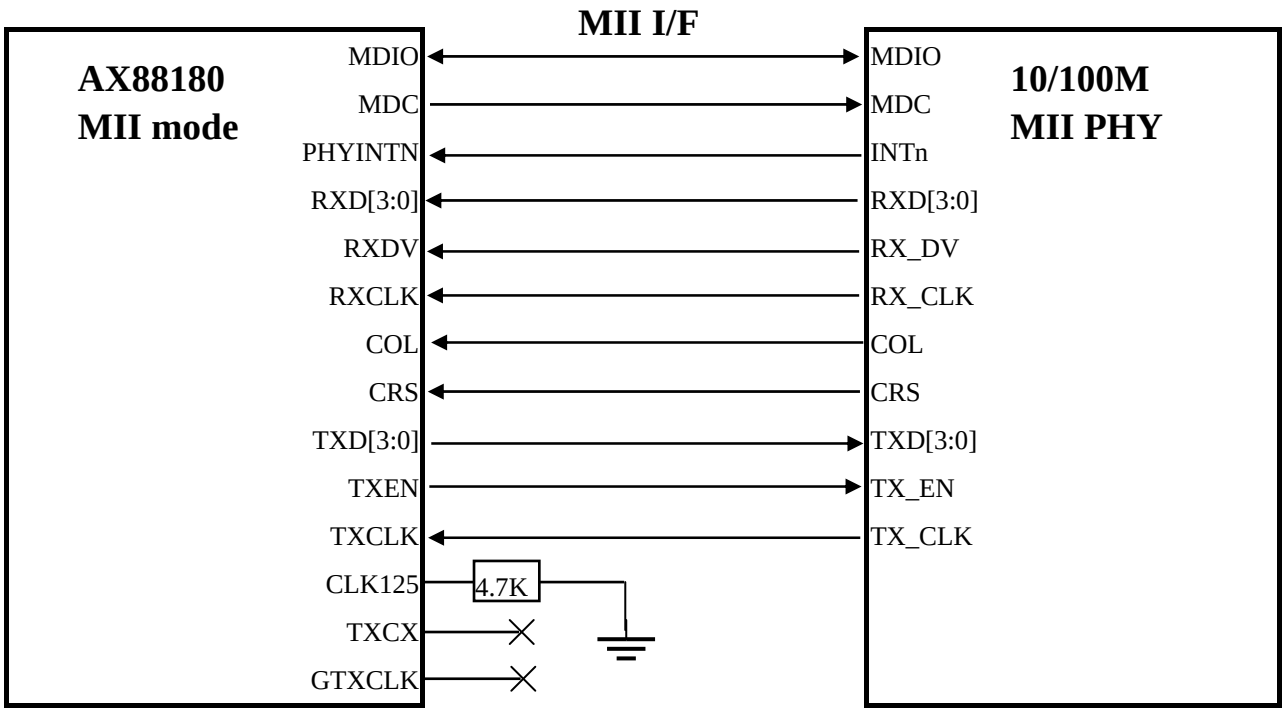


Figure 15. MII Interface Reference Connection

Appendix A5. Synchronous and Asynchronous Timing Selection

AX88180 can support synchronous or asynchronous access from host MCU. Below information provides some references to select clock frequency of host MCU and AX88180.

A5-1. AX88180 is synchronous with host MCU.

The timing selection is suitable for both 32-bit and 16-bit mode. Please refer to Appendix A3 for more details of system design considerations.

Frequency	Access type	Valid access timing (OEN/WEN active timing)
Max 100MHz	Single or Burst	Min 5 reference clocks

A5-2. AX88180 is asynchronous to host MCU.

The timing selection is suitable for both 32-bit and 16-bit mode.

Frequency	Access type	Valid access timing (OEN/WEN active timing)
Max 100MHz	Single or Burst	Min 6 reference clocks (**Note**)

Note: The reference clock is from external OSC and should be synchronously provided to AX88180 HCLK during powering ON the system, and it's not the output of host MCU. For instance, if AX88180 runs in asynchronous mode and refers a 100MHz clock from OSC, whereas MCU runs in 125MHz environment. In such condition, MCU must at least offer 60ns (min 6 reference clocks of 100MHz) access timing to AX88180. The 60ns for MCU is almost reached to 8 clocks (125MHz). We recommend that it is needed to extend the data bus access timing of MCU to meet AX88180's data access timing spec.

Appendix A6. Wake On LAN (WOL) without driver via Magic Packet

A6-1. Wake On LAN (WOL) without driver

AX88180 can support WOL without driver exists. In such situations, system must offer 3.3V voltage, reference clock and rest signal to AX88180. Whenever AX88180 detects magic packet from cable, it will drive WAKEUP signal to host system. AX88180 defaults in MII interface (after reset before EEPROM auto-loaded). Hence if Giga-PHY supports RGMII interface, designer must use EEPROM to set AX88180 to RGMII interface. Users must take care is that AX88180 only supports delay timing of RGMII (refer to 5.5.7), thus it must add extra delay (at least 0.7ns) in PCB board if system needs WOL and without running driver. Below diagram is shown the concept.

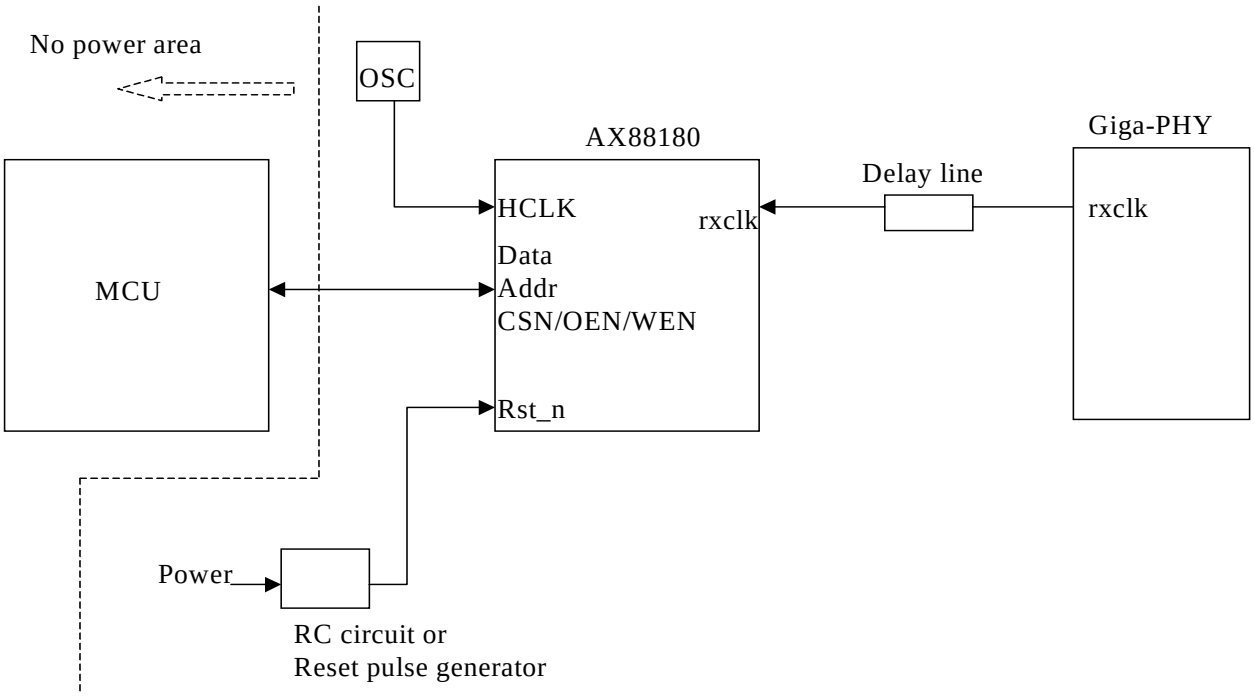


Figure 16. WOL without Driver via Magic Packet

Another available method is to set Giga-PHY in MII mode (by configure pin, if Giga-PHY has this feature). After AX88180 detects magic packet and wakes up system, driver can set AX88180 to RGMII mode and also set Giga-PHY to RGMII mode by MDIO interface. If designer employs this approach, the delay timing issue is not needed.

A6-2. Magic packet

The magic packet received by AX88180 is shown as following;

DA + SA + 0x0000 + 0xFFFFFFFFFFFF + (at least repeats 16 times) DA + CRC32

DA = MAC address of AX88180 (6 bytes)

SA = Source address (6 bytes)

Revision History

Revision	Date	Comment
V1.0	2005/10/04	First edition
V1.0A	2006/03/31	1. Correct some typos in Section 3.4. 2. Correct the name definition of some pins in Section 1-3 and Section 2.
V1.1	2006/07/28	1. Some typo errors corrected between Pin diagram and tables. 2. Host read/write timing revised in Section 5. 3. Some bits of registers are updated. 4. Add some connections between MCU and AX88180 in Appendix. 5. Add wake up LAN in Appendix. 6. Update the power consumption information in Section 5.1.6.
V1.2	2007/03/28	1. Correct some information in Section 3.9 for 16-bit mode operation. 2. Modify the data access timing information in Section 5.2.5, 5.2.6 and Appendix A4. 3. Update the power consumption information in Section 5.1.6. 4. Add some information in Section 3.10. 5. Define the bit filed name (RXJUBOLEN) for bit 10:7 of MAC_CFG1 register. 6. Add AX88180 with Gigabit PHY Connection information in Appendix A3. 7. Modify some descriptions in Section 1.1, 4.6, 4.16, 4.17, 4.18, 4.22, 4.34~4.36, 4.40. 8. Modify the description of TXCLK and GTXCLK pin in Section 2.2. 9. Rearrange the content of Appendix into Appendix A1~A5. 10. Change the number format from 16h'XXXX to 0xXXXX for example.
V1.3	2007/05/04	1. Swap the pin definition of pin #90 and #91 in Section 2.6 and Figure 2. 2. Correct some typo errors of pin type in Table 1 and Table 5.
V1.4	2007/05/18	1. Modify max operation frequency of HCLK from 125MHz to 100MHz. 2. Modify some thermal information in Section 5.1.7.
V1.5	2008/05/05	1. Correct some pin descriptions in Section 2.2, 2.6. 2. Add 125MHz Jitter information in Section 5.2.1. 3. Modify the Host Read/Write timing in Section 5.2.3, 5.2.4, 5.2.5, 5.2.6. 4. Modify Appendix A3 to add the RGMII/MII interface reference connection.
V1.06	2008/06/06	1. Modify the "US Patent Approval" string in the Features page.

V1.07	2008/12/30	1. Modified some descriptions in the Product Description section. 2. Corrected the RGMII Interface Reference Connection diagram in Appendix A3-1. 3. Re-arranged the section numbers in Section 5. 4. Added the power up sequence timing information in Section 5.4. 5. Modified some descriptions in Section 5.5.3, 5.5.4, 5.5.5 and 5.5.6. 6. Added the Tdelay timing and related waveforms in Section 5.5.7 “RGMII Timing”.
V1.08	2010/03/03	1. Modified some descriptions in Section 3.7 and Appendix A5-1. 2. Modified some descriptions in Section 3.8. 3. Updated Figure 4 “data swap block”. 4. Corrected some descriptions of TXBS register in Section 4.6. 5. Modified some descriptions in Section 5.5.3 and 5.5.6. 6. Added Section 5.5.5 “Host Burst Read Timing (16-bit mode)”. 7. Added Section 5.5.8 “Host Burst Write Timing (16-bit mode)”.
V1.09	2010/09/27	1. Modified some descriptions in the Features page. 2. Added more information in the HCLK pin description of Section 2.3. 3. Modified some descriptions in Section 3.10, 4.18 and 4.26. 4. Updated some information in Section 5.5. 5. Re-arranged the contents and added more information in Appendix A1 and A2. 6. Added Appendix A3 to indicate the “System Power Up Reference Clock Design Considerations” information. 7. Modified some descriptions in Appendix A5.
V1.10	2010/11/24	1. Corrected some descriptions in Section 3.10. 2. Modified some descriptions in Section 4.23.

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